

**FSW01-PCI**  
**HIGH –SPEED SWITCHING SIGNAL GENERATOR BOARD**  
**USER’S MANUAL**

**DIGITAL SIGNAL TECHNOLOGY, INC.**

1-6-28, Higashi Benzai, Asaka city, Saitama  
351-0022 Japan

TEL : 81-48-468-6094 FAX : 81-48-468-6210

URL:<http://www.dst.co.jp/>

e-mail:[info@dst.co.jp](mailto:info@dst.co.jp)

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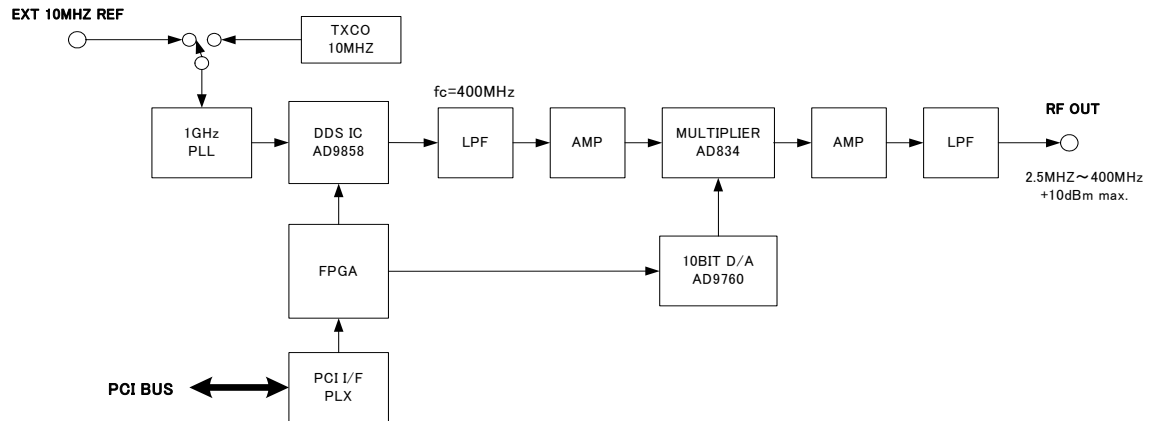
## 1. Function description

FSW01-PCI is a high-speed switching signal generator board with wide band clock source utilizing DDS(Direct Digital Synthesizer) technique. It provides sine wave signal output from 2.5MHz to 400MHz in 0.23Hz step and the frequency can be switched within 1uS. Also, the signal amplitude can be controlled with more than 30dB and switched within 1uS. The output level is maximum +10dBm. Frequency control can be made with PCI-bus inserting to PC PCI slot. In case the accurate 10MHz clock is available externally, the frequency stability can be improved.

## 2. Specifications

Output wave	Sine wave
Output impedance	50 ohm
Output frequency range	2.5MHz - 400MHz
Frequency resolution	about 0.23Hz( $1 \times 10^9 / 2^{32}$ )
Maximum output level	+10dBm $\pm$ 2dB
Output level variable range	more than 30dB
Frequency switching time	within 1uS
Output level switching time	within 1uS
Spurious level	more than 40dBc
Harmonic spurious	more than 20dBc
Interface	PCI bus based on Rev.2.2
Internal clock Frequency accuracy	$\pm$ 1.5ppm
External clock input	10MHz, 0dBm - +6dBm
External clock input impedance	50 ohm
Current	+5V 700mA +12V 450mA -12V 50mA
Dimensions	245x105x20(mm)

### 3. BLOCK DIAGRAM



### 4. THEORY OF OPERATION

1GHz system clock is generated by PLL, using 10MHz reference clock of on-board TCXO or external clock. 1GHz system clock is applied to 32BIT DDS and up to 400MHz sine wave with high frequency resolution is generated by DDS. LPF removes undesired spurious and clock and fed to multiplier where output level is controlled. Output level is controlled by 10bits D/A and over 30dB level control is obtained. Frequency and level control data on PCI bus is fed to FPGA which loads frequency data to DDS and amplitude data to D/A converter. As soon as trigger byte of frequency and(or) level is written, the FPGA immediately writes the data on DDS and D/A and changes the frequency and amplitude within 1uS.

### 5. INSTALLATION OF DEVICE DRIVER

Refer to the attached CD ROM.

### 6. PROGRAMMING

First, write the initial value, Frequency data, Amplitude data in memory region of PCI9030. FSW01-PCI uses only BASE and ADDRESS#2(BAR2) area. Write the data at byte unit. Below is the interface table about OFFSET and register structure of BASE ADDRESS.

OFFSET(hex)	Register	Description	Set value
+0	DDS REG 0x0	AD9858 Registor#0	0x58
+1	DDS REG 0x1	AD9858 Registor#1	0x00
+2	DDS REG 0x2	AD9858 Registor#2	0x00
+3	DDS REG 0x3	AD9858 Registor#3	0x00
+4	DDS REG 0x4	AD9858 Registor#4	0x00
		not used	
+A	DDS REG 0xA	AD9858 Registor#A	FREQ bit0-7
+B	DDS REG 0xB	AD9858 Registor#A	FREQ bit8-15
+C	DDS REG 0xC	AD9858 Registor#A	FREQ bit16-23
+D	DDS REG 0xD	AD9858 Registor#A	FREQ bit24-32
		not used	
+23	DDS REG 0x23	not used	
		not used	
+40	AMP 0-7	AMPLITUDE	AMP bit 0-7
+41	AMP 8-9	AMPLITUDE	AMP bit 8-9
		not used	
+50	TRIG BYTE	bit0: Frequency switching trigger bit1:Output level switching trigger bit2-bit6:not used bit7:H/W reset trigger	
		not used	
+60	BOARD ID	bit0 - bit3: (Read Only bit3=MSB) bit4 - bit7:not used	

#### Remarks

(1) DDS IC is AD9858(Analog Devices). If the special function is not desired, the programming can be done only by writing the above table from +0 to +4 hex.

If desired, please refer to the data sheet of AD9858.

(2)Write "1" to bit 7 of trigger byte before use as it is the internal hardware reset.

(3)Write " 1 " to trigger byte for switching frequency and amplitude(bit0, bit1), and the value of register will be loaded.

(4)The FSW01-PCI board has the ID number to identify the desired board when several boards are installed. ID number is set by DIP SW(S1) on the board.

## **7. How to set the frequency**

As for DDS frequency, write DDS data to A - D(hex) 4 byte. 4 bytes DDS data and output frequency can be derived from the following formula :

$$\text{DDS DATA} = \text{Fout} * 232 / \text{Fclk}$$

Fout : Output frequency(Hz)

Fclk : DDS master clock  $1 \times 10^9$ (Hz)

Change the 32 bits integer found here into binary and write to OFFSET A - D at byte unit. Then, write 01hex to TRIG/BYTE and the desired frequency will be set up.

## **8. How to set the output level**

Apply the output of 10 bit D/A to electrical ATT. See the attached figure of page 7 which shows the output level vs. level data value. Find the value from the curve of the figure and you will see that the output level obtains multiplicative value from two times of the set data. Write the 10 bits amplitude data to OFFSET 40hex,41hex) and then write 02hex to TRG/BYTE.

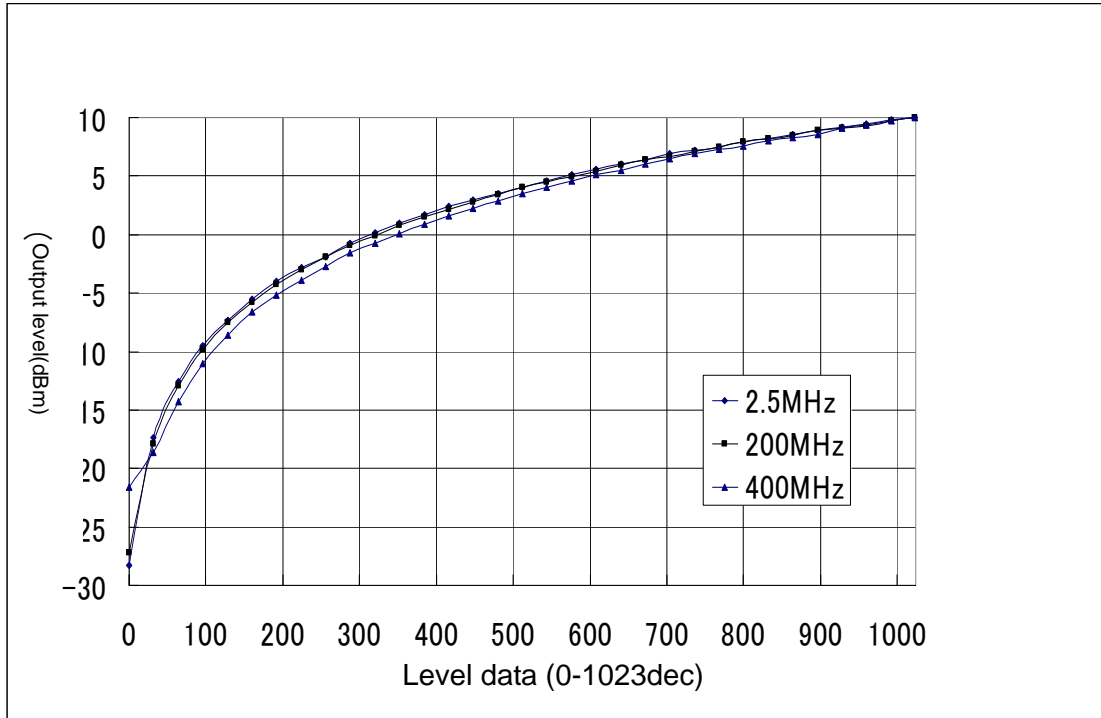
## **9. Sample program**

Refer to the file of an attached CD ROM.

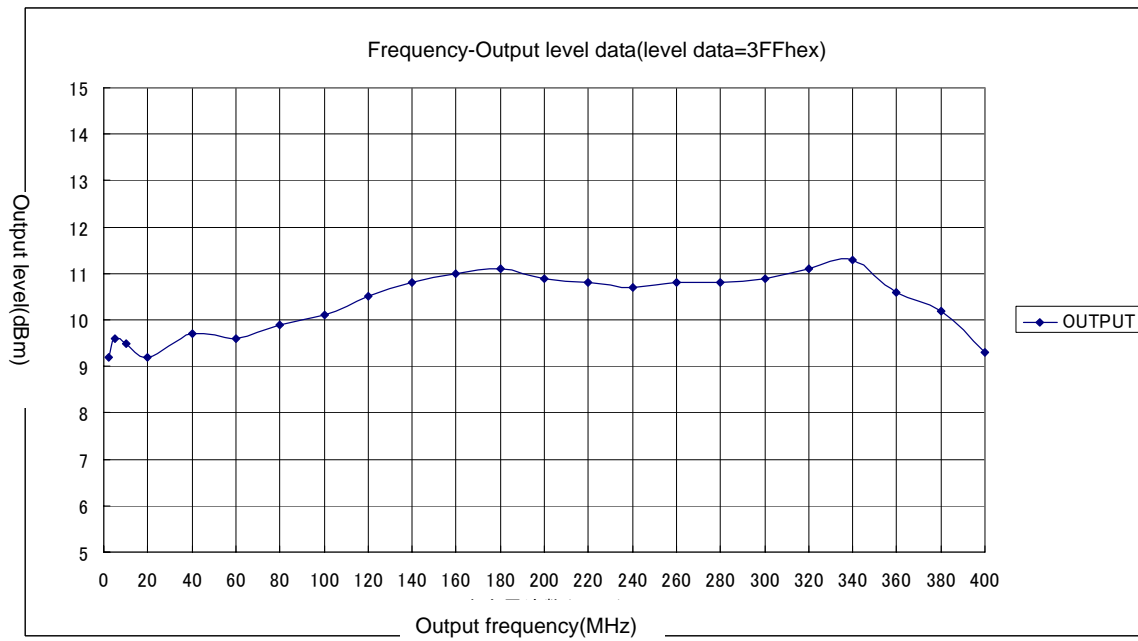
## **10. How to select the reference clock**

Internal TCXO guarantees  $\pm 1.5$ ppm frequency stability. For higher frequency stability, you can use external 10MHz reference source and can obtain the same accuracy as the external one. To change a clock source, short INT of JP3 for the internal clock mode, and short EXT for the external clock mode.

11. FIGURE 1 ( Output level data)



12. FIGURE 2 (Frequency-Output level data)



### **13. Warranty**

There is a one- year guarantee except the case of the damages that may occur as a result of handling by user.

### **14. Cautions**

Handling precaution is required as sensitive CMOS devices are used on the board.

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