PRBS／Pattern Generator

APG-3G

Features

- Independent 2 outputs are provided, which can be set different patterns.
- Maximum bit length：256KBIT.

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Specification

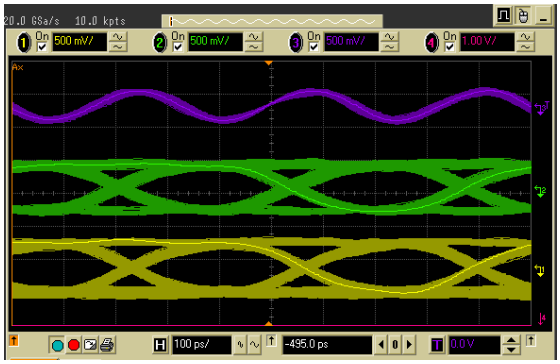
Input clock	SMB connector 50Ω single end AC coupling Sine wave 30MHz-3000MHz -3dBm～3dBm Square wave 2KHz - 3000MHz -3dBm～3dBm Shutdown/Startup time is within 4nS Duty ratio 50±10%
Trigger input	SMB connector 3.3V CMOS Pulled up internally at10 KΩ There is a jitter of +/-5nS up to pattern output start relative to trigger input.
Pattern output	SMB connector Differential PECL 2channels Individual channel patterns can be set Skew between channels is within 20ps
Clock output	SMB connector Differential PECL Skew between patterns is within100pS
Output bit length	(1)External trigger mode Any bit length in a multiple of 32 of 32bit-256Kbits per 1ch (2)Continuous mode Any bit length in a multiple of an even number of 32bit-256Kbits per 1ch
Bit trigger output mode	(1) External trigger mode (2) Continuous mode
Frequency counter	Frequency is counted by internal standard clock. Measurement accuracy is +/-50ppm Measurement range is from 0.1MHz-3040.0MHz.
LED on board	(1) FPGA normal operation display (2) Pattern outputting(also combing with alarm output) (3) Frequency judgment of input RF clock
Control	Asynchronous serial communication 9600bps, 8bit, 1 stop bit, non-parity Signal level 3.3V CMOS
Operating temp. range	0 ～ +60 degree C
Storage temp. range	-30 ～ +70 degree C
Outer dimensions	100mmx 80mm
Power requirements	3.3V single power +/- 0.2V max.1200mA

These products are recommended for your convenience.

PCK3GF-1 can be useful as a clock source.

LVC-232C is available as a level converter between RS-232C such as PC serial port and 3.3V CMOS which is a logic level of APG-3G.

Output wave example



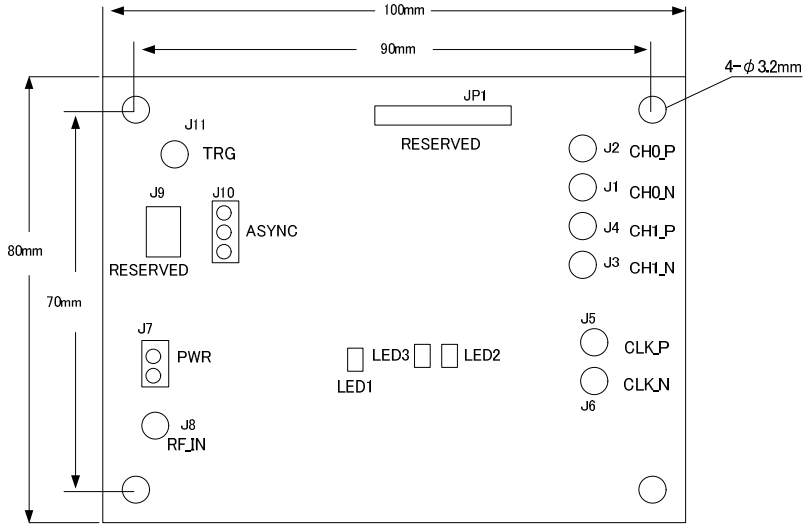
3Gbps PCI Express Compliance pattern

Clock Output

CH0

CH1

Outer dimension



Connector names and description

Connector number	Name	Description
JP1	RESERVED	Not used. This connector must be opened
J1	CH0 N	PECL negative output(SMB) for CHO
J2	CH0 P	PECL positive output(SMB) for CHO
J3	CH1 N	PECL negative output(SMB) for CHO
J4	CH1 P	PECL positive output(SMB) for CHO
J5	CLK P	PECL positive output(SMB) for Clock
J6	CHK N	PECL negative output(SMB) for Clock
J7	PWR	Power supply terminal Part No. DF1BZ-2P-2.5DSA Manufacture: Hirose
J8	REF IN	Clock input(SMB)
J9	RESERVED	Not used. This connector must be opened.
J10	ASYNC	Asynchronous serial communication control Part No. DF1BZ-3P-2.5DSA Manufacture: Hirose
J11	TRG	Input pin under external trigger mode

J7 Connector pin assignment (Part No.DF1BZ-2P-2.5DSA Manufacture: Hirose)

Pin number	Name	Description
1	+3.3V	Supply +3.3V
2	GND	GND

J10 Connector pin assignment (Part No. DF1BZ-3P-2.5DSA Manufacture: Hirose)

Pin number	Name	Description
1	GND	GND
2	RXD	Receiving port(Host→APG-3G)
3	TXD	Transmitting port(Host←APG-3G)