User's Manual

Programmable Oscillator

Model PGN3GF-1

DIGITAL SIGNAL TECHNOLOGY, INC.

1-7-30, Higashi Benzai, Asaka, Saitama, 351-0022 Japan

TEL : 81-48-468-6094 FAX : 81-48-468-6210

WEB : http://www.dst.co.jp/en

email : info@dst.co.jp

Contents

1. General description

PGN3GF-1 is an open framed, non-enclosed signal generator board, equipped PCK3GF-1 and PLL reference clock. REF10MF. PGN3GF-1 can generate any desired clock signals with 1KHz resolution in an extremely wide band of 50MHz to 3000MHz.

2. Specification

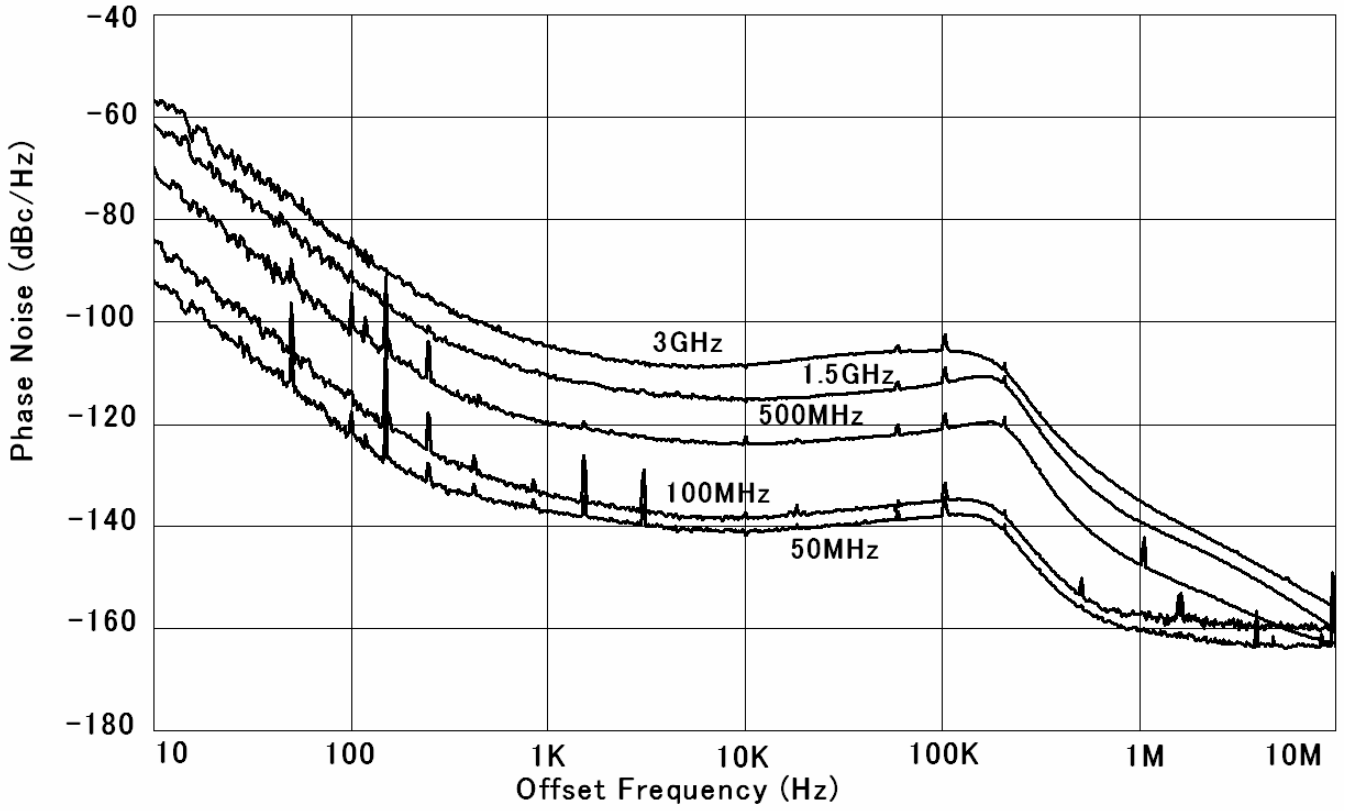
2-1. Electrical specification

1) Output frequency range	50～3000MHz
2) Frequency resolution	1KHz
3) Phase Noise	@3GHz Typical
	10 Hz offset : -55 dBc/Hz Typ.
	100 Hz offset : -85 dBc/Hz Typ.
	1 KHz offset : -104 dBc/Hz Typ.
	10 KHz offset : -105 dBc/Hz Typ.
	100 KHz offset : -105 dBc/Hz Typ.
	1MHz offset : -132 dBc/Hz Typ.
	10MHz offset : -155 dBc/Hz Typ.
	Remarks : The above phase noise is measured with REF10FM reference clock oscillator.
4) Spurious	max -65dBc (except harmonics)
5）Output harmonic level	max -8dBc
6) Output level	+10dBm and more
7) External reference clock and level	10MHz : -6dBm～+10dBm sine wave or square wave
	TTL/CMOS level input possible
8) External reference clock input impedance	1K ohm
9） Lock range on external clock mode	10MHz±25ppm and more
10) Frequency accuracy on internal clock mode	+/-15ppm and less 0 ～ +60 degreeC
11) Unlock output	Lock : High level Unlock : Low level
	3.3V CMOS level
12) Lock time	max 40m sec
13) Interface	(1) USB2.0
	(2) SPI serial communication
	3. 3V CMOS level
	3 byte data (24bit)
14) Power supply	+5V+/-5% max 550mA
15）Dimensions	100x50(mm)

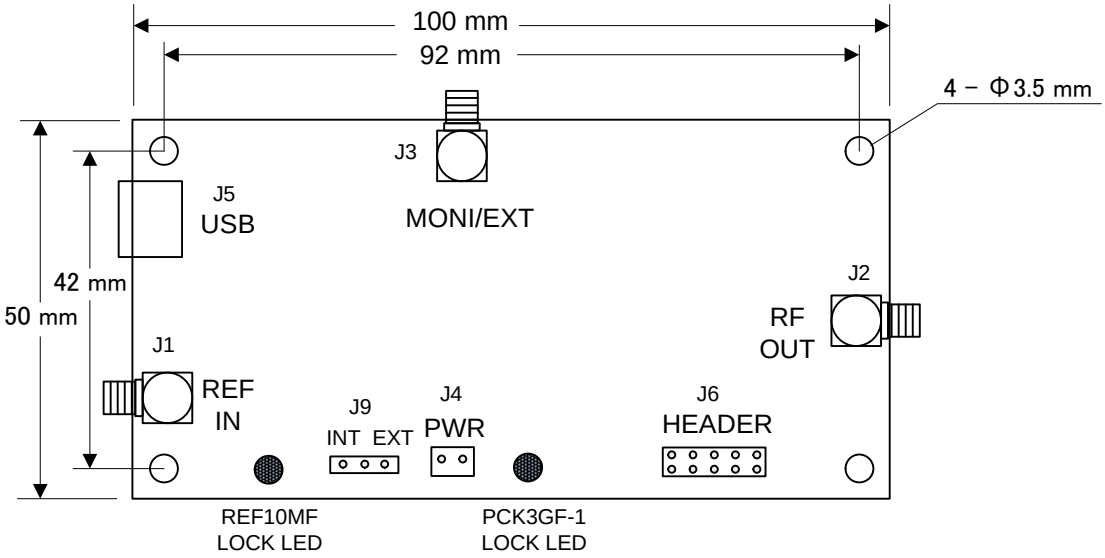
2-2. Environmental condition

1）Operating temperature range	0 ～ +60 degreeC
2）Storage temperature range	-30 ～ +70 degreeC

2-3. Phase Noise



3. Outer dimension



4. Connectors

4-1.Connector Name and description

Number	Name	Description
J1	REF IN	10MHz reference, Output impedance:1K ohm
		Connector : SMA-J
J2	RF OUT	Output pin Connector : SMA-J
		Output impedance : 50 ohm
J3	MONI/EXT	Monitor Output for 100MHz reference clock
		Level : more than 0 dBm(50 ohm terminated)
		Connector : SMA-J.
J4	PWR	Power input +5V
		Connector part number : DF1BZ-2P-2.54DSA(Hirose)
J5	USB	USB interface terminal
		USB part number : USB-Mini-B
J6	HEADER interface	SPI control, Unlock signal, Power supply pin
		Connector : 2.54mm pitch , 5x2 pin header
		Connector part number : PS-10PE-D4T1-PN1(JAE)
J9	EXT/INT	Internal and external switching jumper pin for REF10MF

4-3. J6 Connector pin assignment

Number	Name	Description
1	GND	Power Supply/signal GND
2	GND	Power Supply/signal GND
3	+5V	Power input+5V
		Not using PWR connector, the power can be supplied from here.
4	+5V	the same as above
5	LOCK	PLL lock status output
		3.3V CMOS
6	/CS	Chip select under SPI mode
		Input low active 3.3V CMOS internally pulled up
7	LOCK	PLL lock status output of REF10MF
		3.3V CMOS
8	SDI	Serial clock input under SPI mode
		3.3V CMOS
9	NC	not used
10	CLK	Serial clock input under SPI mode
		3.3V CMOS

5. Control by USB communication

The interface of start/stop synchronization is used by USB communication.

The device is FT232R manufactured by FTDI.

There are two ways to control PGN3GF-1. The one is to control from the virtual COM port of PC and another is to control FT232R directly by user's own program.

5-1. To control settings from the virtual COM port of PC

Procedure 1. Download the FT232R drivers from the link addressed below and then unzip it to a folder.

http://www.ftdichip.com/Drivers/VCP.htm

Procedure 2. Use USB cable to connect J5 and PC. " Found New Hardware Wizard" will begin, and then select the folder where you downloaded. Finally install the driver.

Procedure 3 Set the communication setting of PC as below.

Speed	9600bps
Data bits	8 bits
Stop bit	1 bit
Parity	none
Flow control	none

Any communication software such as Hyperterminal can be used for setting from the virtual COM of PC.

5-1-1. Command definition

Character strings enclosed in double quotation marks " " means ASCII code, and CR and LF, which are control codes, means 0D(hex) and 0A(hex). If any invalid command is entered, "INVALID DATA "CR LF "*" is returned.

All characters used for input should be uppercase. If a normal command is entered, " * " is returned. Also, the entered data is echoed back.

PGN3GF-1 is consisted of PCK3GF-1 and REF10MF but is controlled by SCI serial communication. In case of controlling REF10MF, put always " $ " in front of the command.

5-1-2. Frequency setting command (PCK3GF－1)

For frequency setting, input can be made in MHz, KHz unit.

(1) Setting in MHz

For setting 2450MHz, input the following data.

"2400M"CR

In this case, all the data below 100KHz is set to “0”.

(2) Setting in KHz

For setting 2400002KHz, input the following data.

“2400002K”CR

Also the following expression is allowed.

“2400002”CR

5-1-3. READ command (PCK3GF－1)

By entering “READ”CR, the currently set frequency is output.

The response is as shown below.

“ffffffffKHz”CR LF

“fffffff” is the frequency of currently set in KHz unit.

5-1-4. SAVE command (PCK3GF－1)

By entering “SAVE”CR, the current frequency can be memorized into EEPROM.

When the power is on next time, the stored data can be output.

5-1-5. REF command (PCK3GF－1)

REF frequency can be changed to 50MHz or 100MHz by entering “REF”CR.

The inputted frequency can be memorized into the EEPROM and the last saved frequency can be recalled even if power is off.

The following response is returned.

CURRENT_xxMHz Enter ‘1’ for 50MHz ‘2’ for 100MHz >>

The current REF frequency is displayed on xx. Enter 1 or 2 and the following response is returned.

ARE YOU SURE? Enter “Y”>>

By entering “ Y “ the selected REF frequency stored in the EEPROM will be enabled.

5-1-6. Caution for setting data consecutively (PCK3GF－1)

In case of switching frequency at high speed, data may drop out because the PCK3GF-1 does not use flow control. Upon completion of processing by sending a frequency setting command in 6-3-1, the prompt “*” is returned; therefore, confirm the receiving of this prompt, and then send the next frequency setting command.

5-1-7. Internal clock frequency adjustment command（REF10MF）

Adjust the frequency by entering ”＄ADJ__xxx” CR.

OFFSET is given in xxx with 2' complement HEX data.

Enter 000	for OFFSET 0	
Enter 100	for stepping the frequency up	max 7FF
Enter F00	for stepping the frequency down	max 800

The numeric value itself cannot be converted to frequency, but LSB is appropriated to approximately 2.65Hz. Once frequency is successfully set, it is automatically memorized in EEPROM. And the last saved frequency can be recalled when power is on next time.

5-1-8. STAT command （REF10MF）

By entering "$STAT"CR, the currently set parameters are output, such as internal offset value, PLL lock status and EXT/INT condition.

ADJ=xxx	xxx is SDJ OFFSET value and shows in 2' complement	
LOCK=y	y is the LOCK CONDITION	1: LOCK 0: UNLOCK
EXT/INT=z	z is a CLOCK MODE	1: External clock mode 2: Internal clock mode

5-2. How to control with FT232R by user's own program

1. Download the FT32R driver from the link address below.

   http://www.ftdichip.com/Drivers/D2XX.htm

2. Connect J5 into PC port, and " Found New Hardware Wizard" begins. Select the folder which was done on the procedure 5-1. Then install the driver.

3. Set FT232R in the user's program as the following specification.

Communication speed	9600bps
Data bit	8 bits
Stop bit	1 bit
Parity	none
Flow control	none

Also, refer to the link address below.

http://www.ftdichip.com/Support/Links.htm

6 Control by SPI serial data

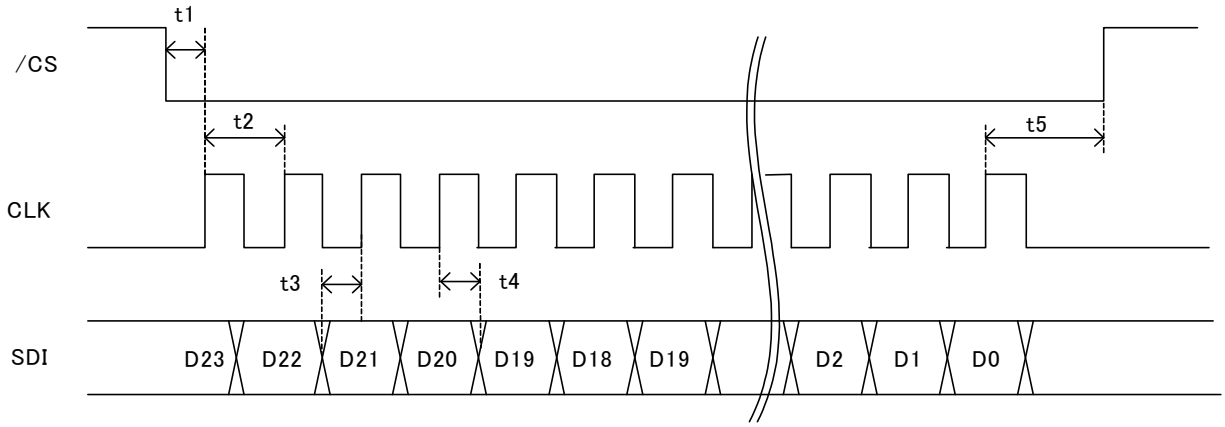
How to set using SPI interface is explained below.

6-1. SPI specification

Max. clock speed	500KHz
Data bits width	24bits (22bits frequency data bits, 2bits reserved)

Logic level 3.3V CMOS

6-2 Timing characteristic



Timing characteristic

Parameter	Condition	Min.	Unit
t1	CLK setup time to /CS	50	ns
t2	CLK period	2	us
t3	SDI setup time to CLK rise edge	100	ns
t4	SDI hold time to CLK rise edge	100	ns
t5	/CS set up time to CLK rise edge	50	ns

6-3. Command definitions

24 bits frequency data is transferred by serial data.

Actual frequency data bits are 22 bits among 24 bits, the remaining 2 bits are not used.

Bit definition is as follows

Bits	Name	Width	Description
bit[23:22]	Reserved	2 bits	Not used, Do not care
bit[21:0]	Frequency	22 bits	Frequency data in 1 KHz resolution in binary

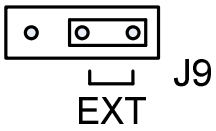
For example, if you set 2456000KHz, frequency data of KHz unit must be converted to binary data.

2456000KHz is converted to 2579C0 hex in 22 bits binary data.

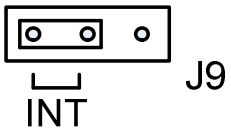
7. How to switch an external clock or Internal Clock

Switching an external clock or internal clock is available at J9.

Jumper under an external clock mode



Jumper under an internal clock mode



8. Shipping inspection

100% inspection shall be performed for the electrical specification in 2-1.

9. Warranty

If any defect is found due to the manufacturer's improper production or design within one year after delivery, repair or replacement shall be performed a the manufacturer's responsibility. DS Technology, Inc. assumes no liability for damages that may occur as a result of handling by users even though the warranty period.

10. Accessories

USB Cable（A – miniB）	1 piece
50cm Power Cable	1 piece

11. Others

11-1. This product, which employs a CMOS device may be easily damaged by static electricity. DS Technology, Inc. assumes no liability for damages that may occur as the result of handling by users even though the above warranty period.

11-2. Do not supply over voltage power supply, module may be damaged. DS Technology, Inc assumes no liability for damages that may occur as the result of handling by users even though the above warranty period.