User's Manual

PLL Reference Clock Oscillator

REF10MF

Digital Signal Technology, Inc.

1-7-30, Hiagashi Benzai, Asaka, Saitama

351-0022, Japan

TEL : 81-48-468-6094 FAX : 81-48-468-6210

WEB : http://www.dst.co.jp/en

email : info@dst.co.jp

Contents

1. General description

REF10MF is a reference clock module utilizing PLL technique which can generate very low phase noise 100MHz VCXO signal. 10MHz is applied to REF10MF as a reference signal.

2. Specification

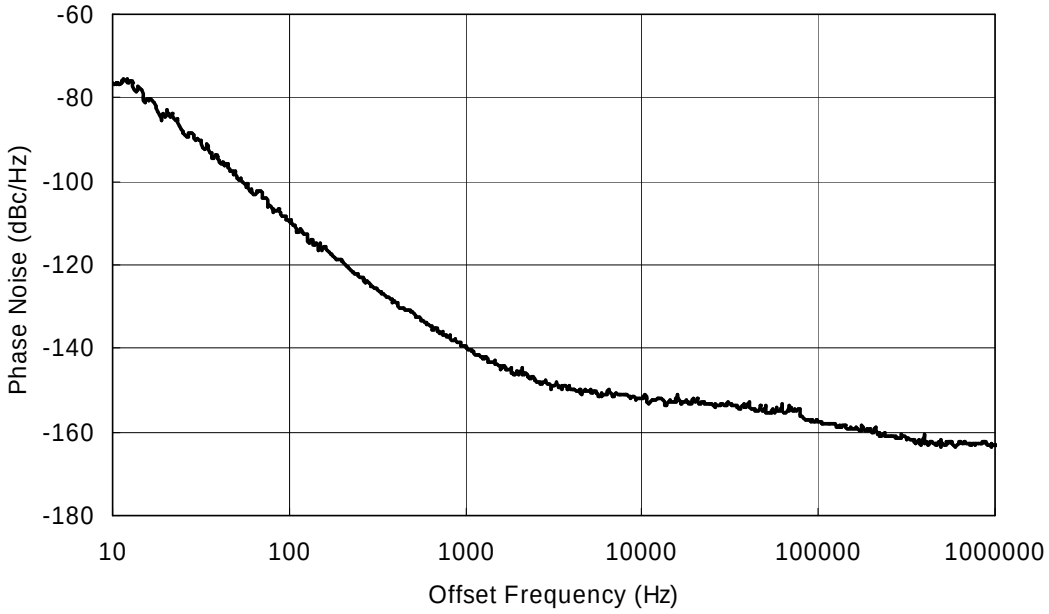
2-1. Electrical specification

1) Output frequency	100MHz	
2) Output port	2 ports	
3) Output level	3.3V CMOS	
5) Phase Noise(Typical)	@3GHz	
	10 Hz offset :	-75 dBc/Hz Typ.
	100 Hz offset :	-109 dBc/Hz Typ.
	1 KHz offset :	-140 dBc/Hz Typ.
	10 KHz offset :	-151 dBc/Hz Typ.
	100 KHz offset :	-157 dBc/Hz Typ.
	1MHz offset :	-163 dBc/Hz Typ.
6) External reference requirement	10MHz	
	(Other frequency except 10MHz is available as an option)	
7) External reference signal level	-6dBm ~ +10dBm sine wave or squire wave	
8) External reference signal input impedance	1K ohm	
9) Spurious	less than -70dBc (except harmonics)	
10) PLL loop band	10Hz	
11) Lock range under the external clock mode	10MHz+/-25ppm and more	
12) Frequency adjustment range under the internal clock mode	100MHz+/-25ppm and more	
13) Frequency accuracy under the internal clock mode	less than +/-15ppm 0 ~+60 degree C	
14) Unlock output	lock: High level Unlock: Low level	
	3.3V CMOS level	
15) Interface	Asynchronous Serial communication	
	9600bps, 8 bits, 1 stop bit, non-parity	
	3.3V CMOS level	
16) Power supply	+3.3V±5% max 100mA	
17) Dimensions	W25.4xD20.32xH7.62(mm)	

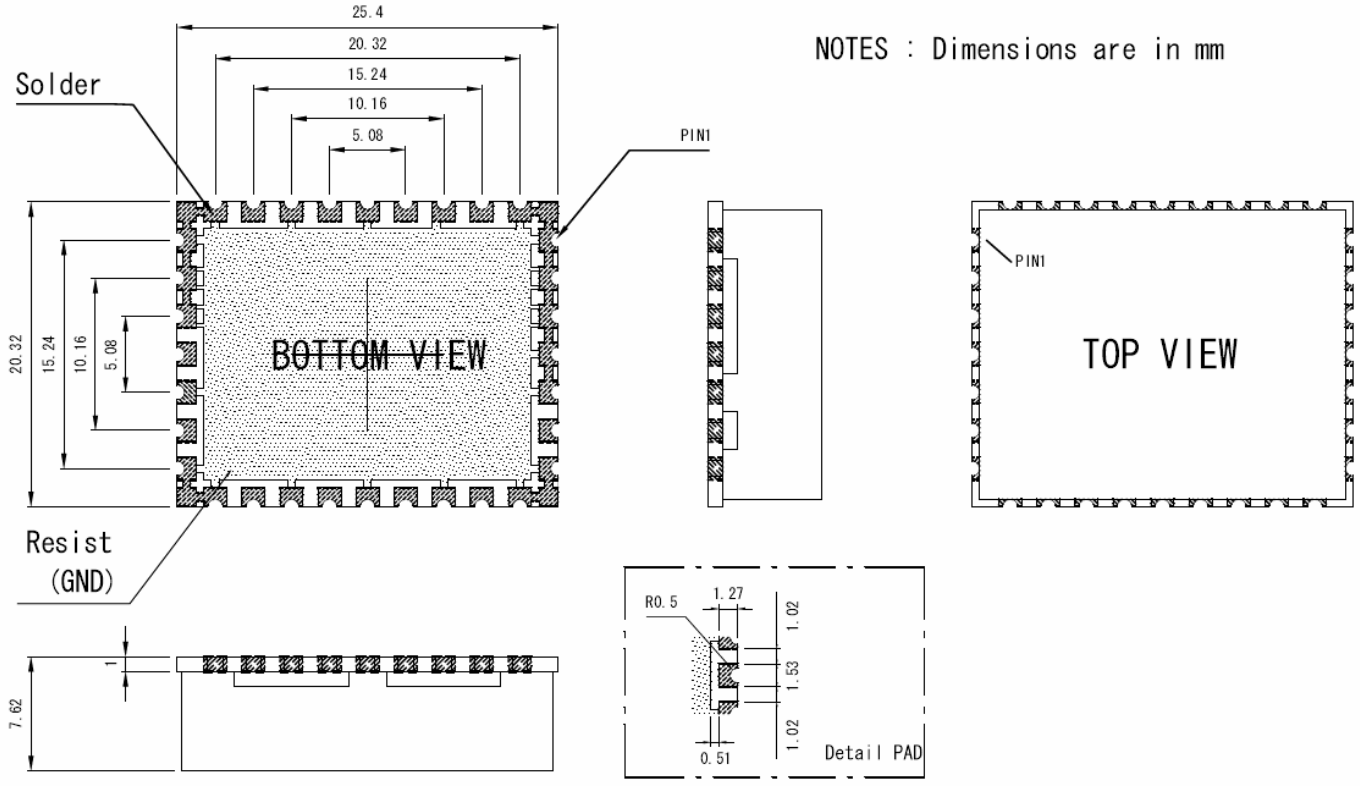
2-2. Environmental condition

1) Operating temperature range	0 ~ +60 degree C
2) Storage temperature range	-30 ~ +70 degree C

2-3. Phase Noise

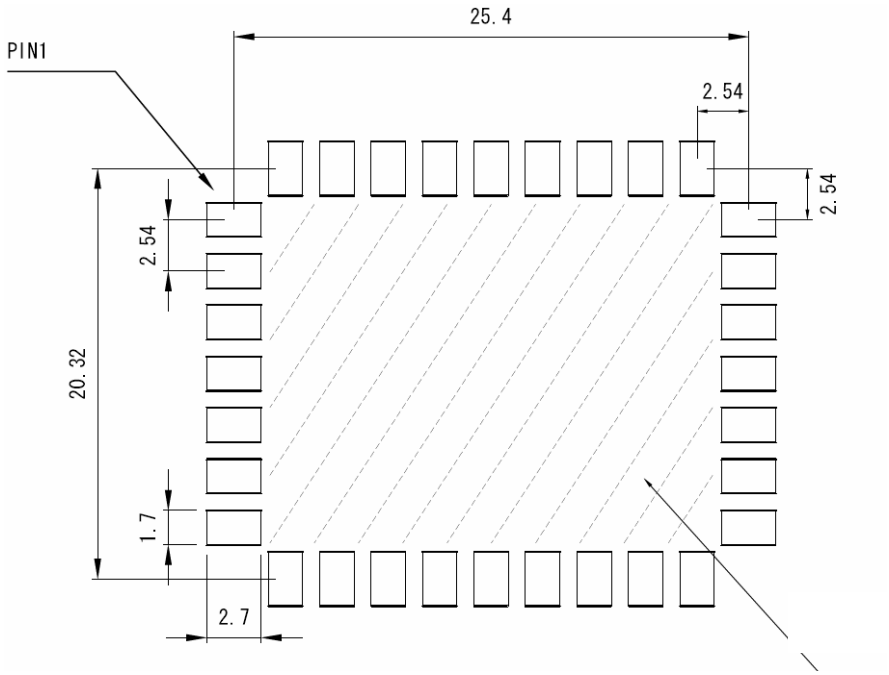


3. Outer dimensions



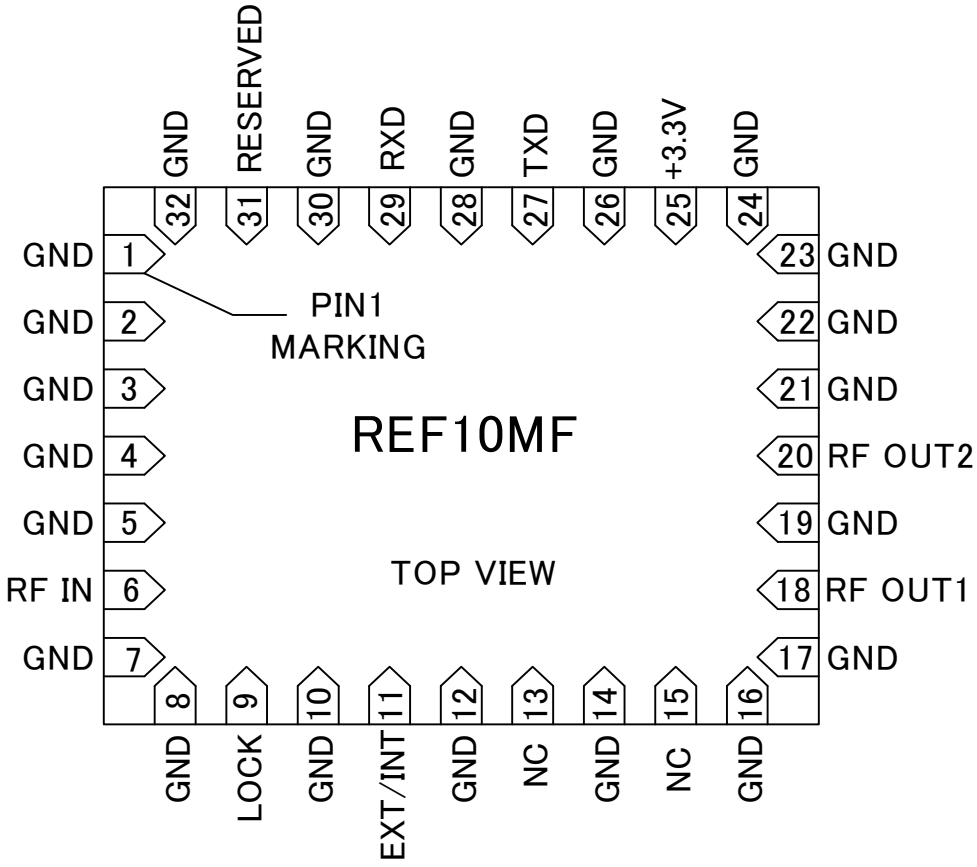
Remarks : The bottom covered by the resist is GND.

4. The recommended footprint as below



The recommended footprint

5. Pin assignment



6. Pin names and description

Pin.	Name	Description
6	REF IN	10MHz reference　1K Ohm
9	LOCK	PLL lock status output High: lock　Low: Unlock 3.3V CMOS
11	EXT/INT	Mode selection pin External or Internal High: External　Low: Internal Internally pulled up
13	NC	not used
15	NC	not used
18	RF OUT1	Output pin 100MHz
20	RF OUT2	Output pin 100MHz
25	+3.3V	Power input +3.3V
27	TXD	Asynchronous serial TX data 3.3V CMOS
29	RXD	Asynchronous serial RX data 3.3V CMOS Internally pulled up
31	RESERVED	Reserved pin. This pin must be opened.

** Other pins are all GND.

pin1-5,7,8,10,10,12,14,16,17,19、21-24,26,28,30,32.

7. Control by Asynchronous serial data

How to set from a PC serial port.

7-1. Communication specification

Speed	9600bps
Data bits	8 bits
Stop bits	1 bit
Parity	none
Flow control	none
Logic level	3.3V CMOS レベル

7-2. RS-232C connection

The logic level of PCK3GF-1 serial communication is 3.3V CMOS, which cannot be directly connected to RS-232C level like PC serial port. Level converter(LVC-232C) between RS-232C and 3.3V CMOS is needed.

LVC-232C is available from our products line-up. Refer to our Web site

7-3. Command definitions

Character strings marked as double quotation marks "means ASCII code, and CR and LF, which are control codes, means 0D(hex) and 0A(hex). If any invalid command is entered, "INVALID DATA"LF CR"*" is returned. All characters used for input should be uppercase. If a normal command is entered, "*" is returned. Also the entered data is echoed back.. "_(underbar)" means space, 20(hex).

7-3-1. Internal clock frequency adjustment command

Adjust the frequency by entering "$ADJ_xxx"CR.

OFFSET is given in xxx with 2' complement HEX data.

Enter 000 for OFFSET 0

Enter 100 for stepping the frequency up max 7FF

Enter F00 for stepping the frequency down max 800

The numeric value itself cannot be converted to frequency, but LSB is approximately 2.65Hz. Once frequency is successfully set, it is automatically memorized into EEPROM. At the next power on, the last entered frequency is retrieved.

7-3-2. STAT command

By entering "$STAT"CR, the currently set parameters are output, such as internal offset value, PLL lock status and EXT/INT condition..

ADJ=xxx xxx is ADJ OFFSET value and shows in 2' complement.

LOCK=y y is the LOCK CONDITION. 1 : LOCK 0 : UNLOCK

EXT/INT=z z is a CLOCK MODE. 1 : External clock mode 2 : Internal clock mode

8. Shipping inspection

100% inspection shall be performed for the electrical specification in 2-1.

9. Soldering condition

Peak temperature : 240 degree C

Soldering time: less than 10 second at the peak temperature

10. Warranty

If any defect is found due to manufacture's improper or design within one year after deliver, repair or replacement shall be performed at the manufacturers responsibility. Digital Signal Technology assumes no liability for damages that may occur as a result of handling by users even though the warranty period.

11. Others

10-1. This project, which employs CMOS device, may be easily damaged by static electricity, Digital Signal Technology assumes no liability for damages that may occur as a result of handling by users even though the above warranty period.

10-2. Do not supply over voltage power supply, or the module may be damaged. Digital Signal Technology assumes no liability for damages that may occur as a result of handling by users even though the above warranty period.

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