FSW01
HIGH-SPEED SWITCHING SIGNAL GENERATOR BOARD

USER'S MANUAL

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CONTENTS

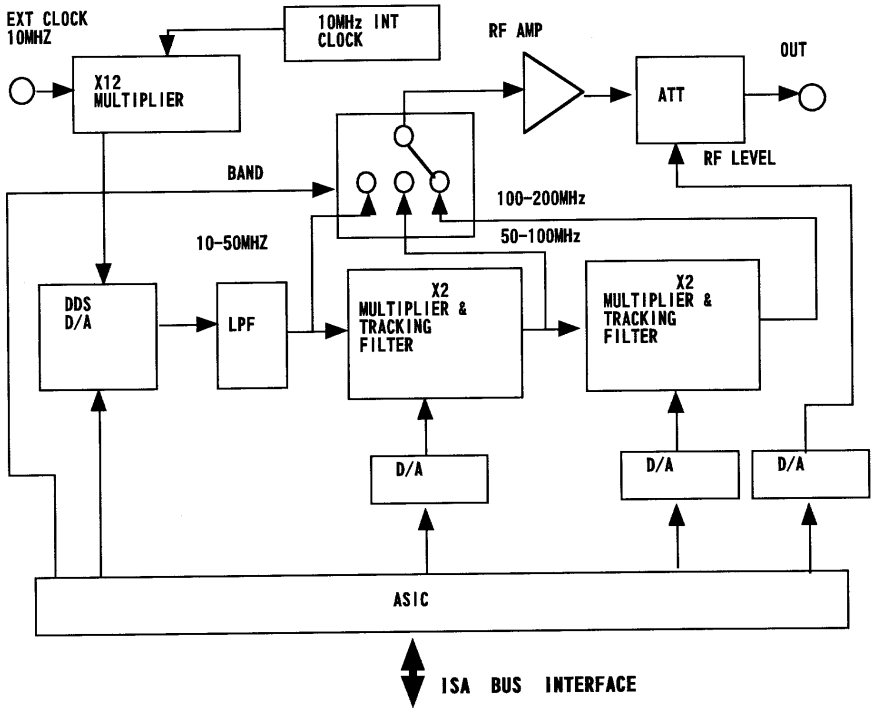
1. FUNCTION DESCRIPTION

FSW01 is a high-speed switching signal generator board utilizing DDS technique and high-speed tracking band pass filter. It provides sine wave signal output from 10MHz to 200MHz in 0.1Hz step and the frequency can be switched within 1uS. Frequency control can be made with ISA-BUS inserting to PC ISA slot. It is possible to use parallel port of micro controller because of 8 bit data bus. When an accurate 10MHz is available externally, frequency stability can be improved and synchronous operations can be possible.

2. SPECIFICATIONS

Output wave	Sine wave
Output impedance	50Ω、SMA connector
Output frequency range	10MHz ～ 200MHz
Frequency resolution	about 0.1Hz
Maximum output level	+10dBm ±3dB
Output level variable range	more than 30dB
Frequency switching time	within 1uS
Output level switching time	within 10uS
Spurious level	more than 40dBc
Harmonic spurious	more than 30dBc
Interface	ISA BUS (8 bit)
Frequency accuracy	Internal clock: ±20ppm(0～+50℃) External clock : according to external clock accuracy
External clock input	10MHz, more than 1vp-p, SMA connector
Current	+5V: 300mA +12V: 450mA -12V: 30mA
Operational temperature	0～+50℃
Dimensions	255x107x20(mm)

3. BLOCK DIAGRAM



4. THEORY OF OPERATION

DDS generates 10~50MHz signal, and its output frequency is multiplied by 2 of 4 using one or two stages of x2 multipliers. Outputs of those multipliers or DDS is selected by high-speed sw and amplified to +10dBm level.

Tuning voltage of the tracking band pass filter can be controlled by D/A converter. When frequency is changed, it tracks the desired center frequency.

The output level can be controlled from -20dBm to +10dBm using electrical attenuator and 10 bit D/A converter.

The internal or external 10MHz clock signal is multiplied by 12, and 120MHz clock is fed to DDS as a master clock.

5. INTERFACE SPECIFICATION

FSW01 uses only signal pins of ISA-BS as below;

ISA-BUS

pin no.	name	spec	
A2	SD7	bi-directional 8 bits data bus	bit7
A3	SD6	bi-directional 8 bits data bus	bit6
A4	SD5	bi-directional 8 bits data bus	bit5
A5	SD4	bi-directional 8 bits data bus	bit4
A6	SD3	bi-directional 8 bits data bus	bit3
A7	SD2	bi-directional 8 bits data bus	bit2
A8	SD1	bi-directional 8 bits data bus	bit1
A9	SD0	bi-directional 8 bits data bus	bit0
A11	AEN	input, low active,register select	
A16	SA15	input, address bus	bit15
A17	SA14	input, address bus	bit14
A18	SA13	input, address bus	bit13
A19	SA12	input, address bus	bit12
A20	SA11	input, address bus	bit11
A21	SA10	input, address bus	bit10
A22	SA9	input, address bus	bit9
A23	SA8	input, address bus	bit8
A24	SA7	input, address bus	bit7
A25	SA6	input, address bus	bit6
A26	SA5	input, address bus	bit5
A27	SA4	input, address bus	bit4
A28	SA3	input, address bus	bit3
A29	SA2	input, address bus	bit2
A30	SA1	input, address bus	bit1
A31	SA0	input, address bus	bit0
B1	GND	power supply、GND	
B2	RESET	input, high active, initialize internal registers	
B3	+5V	power supply、 +5v	
B7	-12V	power supply、-12V	
B9	+12V	power supply、+12V	
B10	GND	power supply、GND	
B13	-IOW	input, low active register write enable	
B14	-IOR	input, low active, register read enable	
B29	+5V	power supply、+5V	
B31	GND	power supply、GND	

Refer to IBM PC technical reference for the ISA-BUS details.

6. PROGRAMMING

There are several registers in FSW01 to set up the frequency. The setting of the frequency and the amplitude must be set up FSW01 register properly. Even FSW01 resisters can be read or written,but programming can be made only writing resisters.

6—1. Setting up a base address

The base address of the register of the I/O space can be selected by DIP SW on the board.

BASE ADDRESS	DIP SW setting			
	1	2	3	4
0300H	X	X	0	0
0400H	X	X	0	1
0800H	X	X	1	0
0C00H	X	X	1	1

1:ON 0:OFF x:do not care

6—2. A structure of register

OFFSET	register	spec	
+0	D0-D7	DDS frequency data	bit0-7
+1	D8-D15	DDS frequency data	bit8-15
+2	D16-D23	DDS frequency data	bit16-23
+3	D24-D31	DDS frequency data	bit24-31
+4	A0-A7	output level data	bit0-7
+5	A8-A9	output level data	bit8-9
+6	TRIG/BAND	bit0: frequency switching trigger	
		bit1: output level switching trigger	
		bit2: frequency band SW0	
		bit3: frequency band SW1	

Remarks: Setting "1" on TRIG/BAND register, the switching activation can be triggered by the falling edge of -IOW signal.

6—3. How to set the frequency

An output frequency is determined by DDS frequency and number of multipliers. 1 time, 2 times and 4 times can be chosen by setting the frequency band bits. 32 bits frequency data of DDS can be derived from the following formula;

DDS DATA＝Fout＊2^{32}／Fclock／multiple

Fout:	output frequency(Hz)	
Fclock:	DDS master clock 120x10^6(Hz)	
multiple:	will be decided by SW0、SW1 bits	1、2、4
	10MHz～50MHz : nultiple＝1	
	50MHz～100MHz : multiple＝2	
	100MHz～200MHz : multiple＝4	

The 32 bits integer found here is changed into binary, and the total 4 bytes of d0-d7, d8-d15, d16-d23, d24-d31 are set up at byte unit.
The frequency switching activation is made by writing "1" to the bit 0 of TRIG/BAND.

6—4. How to set the output level

The output of 10bit D/A is applied to electrical ATT. See the attached figure which shows the output level v.s. 10bit D/A value.
Find the value from the curve of the figure and divide into a lower eight bits and an upper two bits then set the two bytes of A0-A7, A8-A9 at byte unit.
The output level switching activation can be made by writing "1" to bit 1 of TRIG/BAND.

6—5. How to set trigger and band

A frequency and an output level is changed individually or at the same time by writing "1" to trigger bit. If this bit is cleared, the setting up of the next data becomes possible. There is no need to make sure whether the frequency and level trigger bits is cleared , because it is cleared within 1uS after set up.

Setting "1" on this register, the switching activation can be triggered by the falling edge of -IOW signal.

Refer to the table shown below for the relations between the output frequency and the band. The following 3 bands are selected by the bit of SW0, SW1.

output frequency	SW1	SW0	spec
10MHz～50MHz	0	1	multiple of DDS x 1
50MHz～100MHz	1	0	multiple of DDS x 2
100MHz～200MHz	1	1	multiple of DDS x 4
output OFF	0	0	output off

6—6. Caution of programming

Write register at byte unit because it is a 8 bit data bus.
Do not write at word unit.

7. EXTERNAL CLOCK MODE

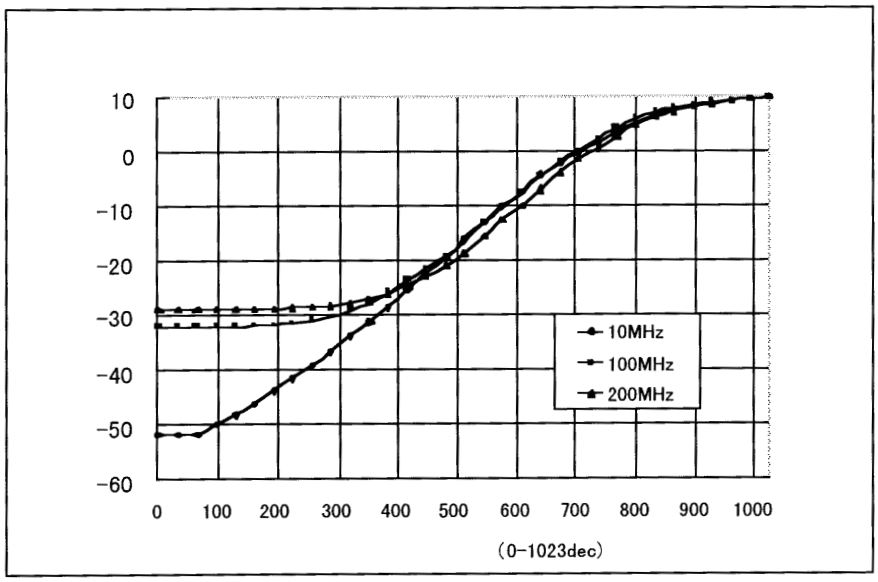
It is possible that the frequency accuracy is made equal to the external clock source. The external clock mode is enabled by setting DIP SW BIT 1 to ON. It becomes possible that the synchronous signals are generated on more than one board when the external clock mode is used.

8. Cautions

(1) As there are unwanted sources of noise in the inside PC, spurious character of FSW01 sometimes deteriorates.

(2) In case the external clock has been stopped on external clock mode,unexpected frequency is generated.

9. Output level data



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