PCK-80 UNIVERSAL CLOCK

USER'S MANUAL

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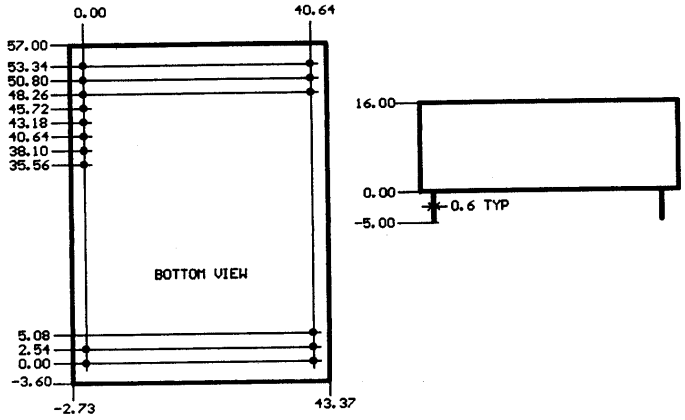
Function Description

The PCK-80 can generate wide band clock signal(at 1Hz resolution) from 1Hz to 80MHz. The signal is generated using 32 bits DDS (Direct Digital Synthesizer) and is with high stability and purity.
Frequency setting is made using parallel data such as BCD SW or, can be made through RS-232C port of PC by serial data.
A frequency can be memorized into the EEPROM and in case of setting the power off, and on again, the stored frequency can be output.
Frequency accuracy can be obtained in external clock mode applying 10MHz clock.

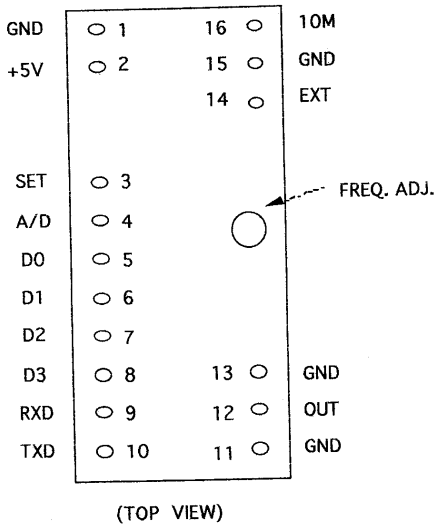
Electrical Specifications

Power requirement		
Supply voltage		+5V ± 5%
Current		300mA
Output level		TTL compatible CMOS level
Output frequency range		1Hz ~ 80,000,000Hz
Frequency resolution		1Hz
Output wave duty		1Hz-40MHz 50% ± 10% 40MHz-80MHz 50% ± 20%
Frequency accuracy		Internal clock : ± 20ppm, 0°C−50°C (adjustable) External clock : depends on external clock accuracy
Phase noise		<-90dBc at 1KHz offset
Spurious		1Hz - 15MHz more than -50dB 15MHz - 30MHz more than -40dB 30MHz-60MHz more than -36dB 60MHz-80MHz more than -32dB(except harmonics)
Frequency save times		more than 10,000 times
Frequency control		
	Parallel input	Six(6) control pins 4-bit BCD input, 1 bit digit/data selection 1 bit strobe signal
	Serial input	two(2) data pins 9600 BPS, 8 bit w/o parity 1 stop bit, ASCII 8 digit numeric data and carriage return code
External clock input		10MHz(TTL or CMOS)
Frequency switching time		within 2mS(time from end of data loading)
Dimensions		61 x 46 x 16mm

OUTLINE



PIN ASSIGNMENT



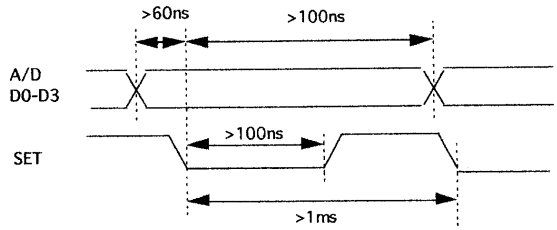
(TOP VIEW)

PIN DESIGNATION AND DESCRIPTION

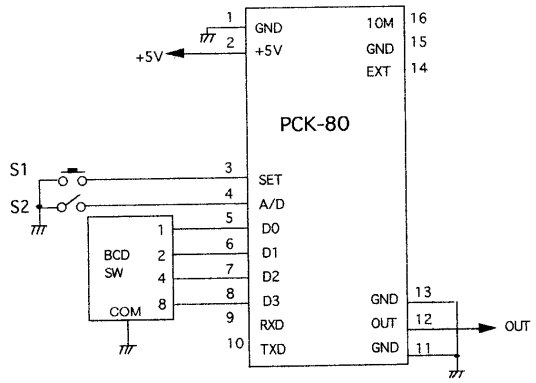
Pin Number	Designation	Description
1	GND	GND of power supply and signal
2	+5V	Power supply pin. Supply +5V ±5%
3	SET	Strobe signal to set by parallel data, pulled-up internally, the data of A/D, D0-D3 can be read into by falling edge of this signal
4	A/D	Select the digit or value of parallel data D0-D3. Select the digit to be changed from the 8-digit frequency data, with A/D pin high(open). Set the value of selected digit with A/D pin low(short to GN). Pulled-up internally.
5	D0	Input of bit 0(2^0) of frequency data digit on value data. Internally pulled-up, 0 for H(open), 1 for L(short to GND) due to complimentary input.
6	D1	Input of bit 1(2^0) of frequency data digit or value data.
7	D2	Input of bit 2(2^1) of frequency data digit or value data.
8	D3	Input of bit 3 (2^2) of frequency data digit or value data.
9	RXD	A synchronous serial RX data, CMOS level compatible to TTL. Input is pulled-up, keep open when not used.
10	TXD	A synchronous serial TX data, CMOS level compatible to TTL. Keep open when not used
11	GND	GND of power supply and signal
12	OUT	Pin of output signal
13	GND	GND of power supply and signal
14	EXT	External clock enabled pin. Connect to H(+5V) in order to operate by external clock. Internally pulled-down, make it open in order to operate by internal clock
15	GND	GND of power supply and signal
16	10M	External clock input pin. In the external clock mode, apply an accurate 10MHz external clock to this pin.

the frequency data,this process cannot be done in time,if frequency setting is made in consecutive condition. One frequency has been set, wait 1mS to set new frequency(refer to the following timing chart.

Parallel data timing chart



Circuit example by Parallel data



Use complimentary type for BCD SW.

Function Table

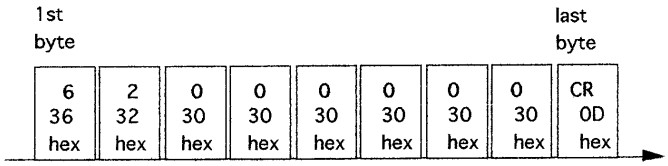
A/D	D3	D2	D1	D0	FUNCTION
L	L	L	L	L	Frequency Data 0
L	L	L	L	H	Frequency Data 1
L	L	L	H	L	Frequency Data 2
L	L	L	H	H	Frequency Data 3
L	L	H	L	L	Frequency Data 4
L	L	H	L	H	Frequency Data 5
L	L	H	H	L	Frequency Data 6
L	L	H	H	H	Frequency Data 7
L	H	L	L	L	Frequency Data 8
L	H	L	L	H	Frequency Data 9
H	L	L	L	L	Set 1 Hz digit
H	L	L	L	H	Set 10Hz digit
H	L	L	H	L	Set 100Hz digit
H	L	L	H	H	Set 1KHz digit
H	L	H	L	L	Set 10KHz digit
H	L	H	L	H	Set 100KHz digit
H	L	H	H	L	Set 1MHz digit
H	L	H	H	H	Set 10MHz digit
H	H	L	H	L	Memory frequency

H : open L : short to GND

Input Data of D0-D3 and A/D is taken into at the set's fall edge.

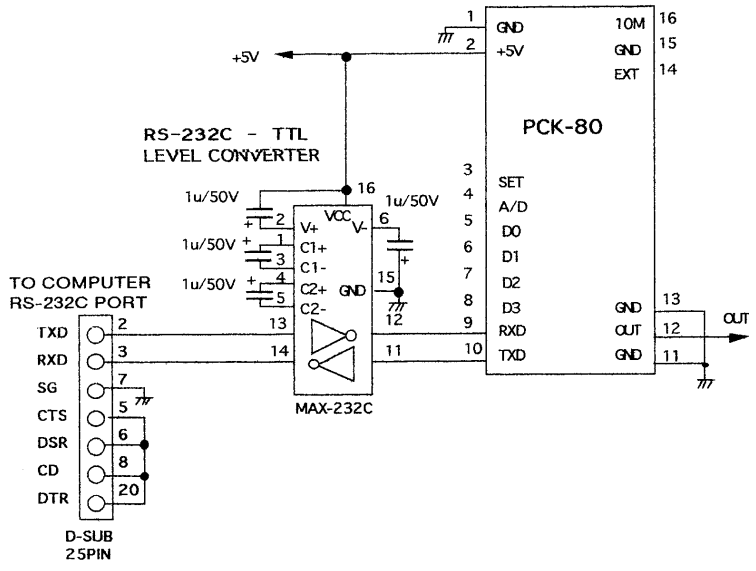
(2) Setting frequency by serial data

In order to set the frequency using a synchronous serial data, frequency data is to be transferred under the format shown below. When the PCK-80 received the data correctly and complete the frequency setting, it returns "*" code (24 hex) as a prompt. When the data received in-correctly or some errors occurred during the transfer, it returns "INVALID DATA". Also ASCII data input from RXD is echo-backed to TXD, and it is confirmed that the transfer is done correctly in due course. Flow control is not made especially, however, there is no problem in transferring the data continuously. The following table shows the data inputting 62,000,000Hz.



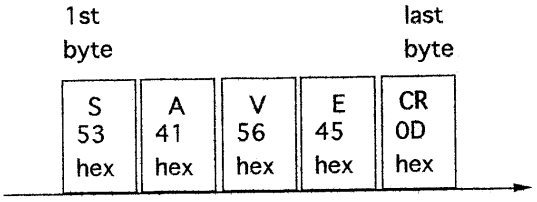
In case input frequency data is less than 8 bytes, the upper byte not-input is regarded "0", and when setting "62000", the frequency is set at 62KHz.

Serial data frequency setting circuit example



<How to memorize the frequency from serial port>

In order to memorize the frequency into the built-in EEPROM, "SAVE"command shown in the following chart if transferred. "EEPROM SAVED!"message is returned,if the data is correctly written.



Sample programming example using serial data

Programming sample in BASIC, using PC and realizing the sweep generator sweeping 100KHz to 80MHz by 100KHz step is under-mentioned.

```
10      OPEN "COM1:9600,N,8,1"AS #1
20      FOR FREQ = 1 TO 800
30      D$=STR$(FREQ)
40      C$=MID$(D$,2,8)+"00000"
50      PRINT C$
60      PRINT #1,C$
70      C$=INPUT$(LOC(1),#1)
80      NEXT FREQ
90      END
```

ALIGNMENT PROCEDURE TO OPERATE BY EXTERNAL 10MHz CLOCK

In case the accurate 10MHz clock is available externally,the synchronizing frequency to the clock can be obtained. In this case, please use the signal source having the frequency accuracy of less than 10MHz ±10ppm. This is to lock the built-in clock of PCK-80 using the external signal.

In the other hand, alignment is required to get the stable clock in using external clock. This alignment requires to turn the trimmer for frequency alignment under the condition of giving external clock in order to lock in a stable condition. This alignment requires a oscilloscope. Following is to show the alignment procedure using the external clock mode.

ALIGNING METHOD

(a)Add the external 10MHz to 10MHz pin of PCK-80, and add +5V to the external clock pin.
(b)Set frequency at 10MHz, connect the PCK-80 output to the CH.1 of oscilloscope to display the wave form.

(c)Connect the external 10MHz clock to the extra trigger or CH2, input of oscilloscope and adjust the trigger level to make synchronization.
(d) Turn the trimmer of PCK-80 for the frequency alignment, and align to the point where the wave form comes to stopped.

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