UPL-240

UNIVERSAL PLL

USER'S MANUAL

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Function Description

UPL-240 is wideband oscillator utilizing high performance PLL(Phase Locked Loop). It can generate signal from 4.5MHz – 240MHz frequency phase locked with external or internal clock. Output frequency can be calculated : Fout=Fin*N/R simply setting R and N value. The frequency can be controlled by parallel data such as BCD SW or serial data which can be connected to PC communication port. Setting values can be stored into the EEPROM and the stored values can be retrieved even power is turned off. Phase adjustment capability enables to make desired phase delay to the external reference clock. Clock signal which is video line(H-sync) locked can be generated when reference divider is set to "1".

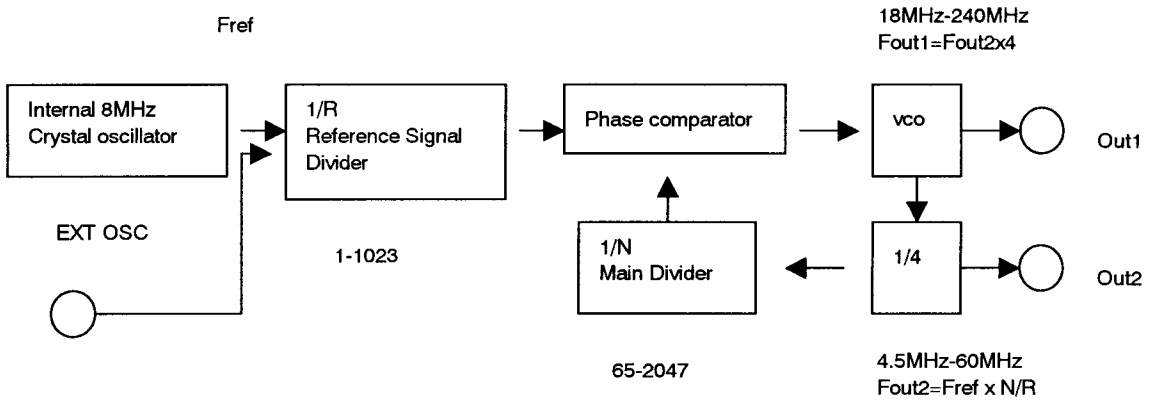


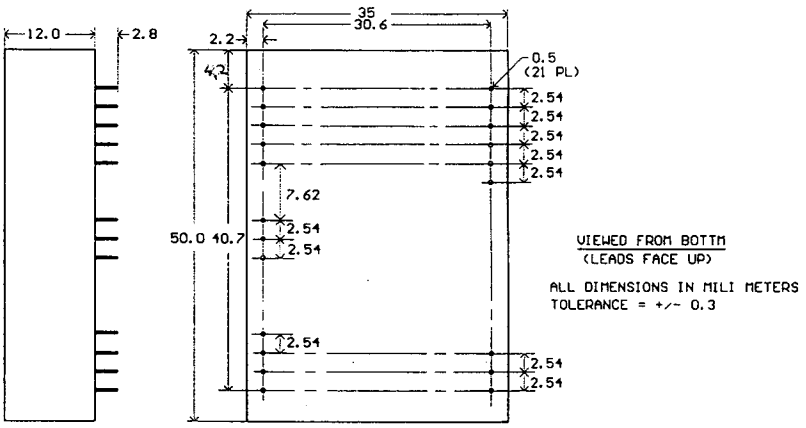
Figure 1 Functional Block Diagram

Electrical Specifications

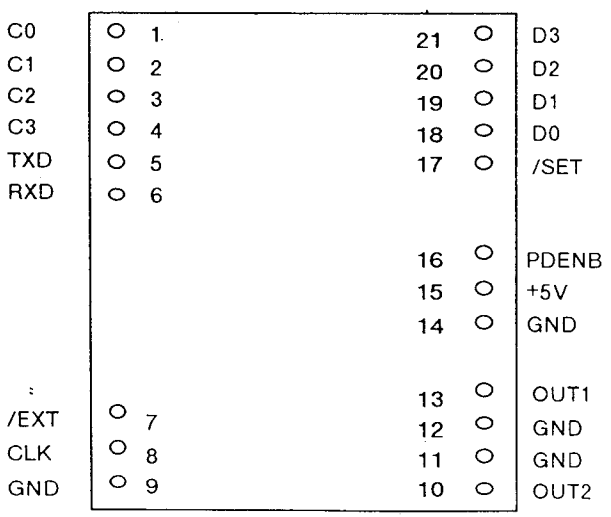
Power supply/current	+5V±5%, 60mA
Output level	OUT1: more than 1.5Vp-p without load (with 50Ω termination: more than 0.75Vp-p) OUT2: TTL/CMOS
Output frequency range	OUT1: 18MHz – 240MHz OUT2: 4.5MHz – 60MHz(1/4 of OUT1 frequency)
Phase comparator freq. range	10KHz- 200KHz
Output wave duty	OUT1 : 50%±20% OUT2 : 50%±5%
Jitter	Phase comparator freq. 10KHz: less than ±10nS (OUT2) Phase comparator freq. 100KHz: less than ±2nS (OUT2)

External clock freq.range	10KHz – 25MHz
Frequency accuracy	Internal : ±50ppm (0°C~50°C)
	External: depends on external clock accuracy
Spurious	less than –30dB(except harmonics)
Reference divider range	1-1023
Output main divider range	65-2047
Output phase	0° /90° /180° /270° (OUT2)
Fine phase control	max.10-15nS , resolution is approx. 1nS
Non-volatile memory save time	more than 10,000
Frequency control	Parallel input: 9 control pins. 4 bits BCD input,
	Serial input two(2) data pins signal level TTL:
	9600BPS, 8 bit, w/o parity 1 stop bit
	ASCII 7 digit numeric data and carriage return code
Frequency switching time	300mS
Dimensions	50x35x12mm

■ Outline



■Pin assignment



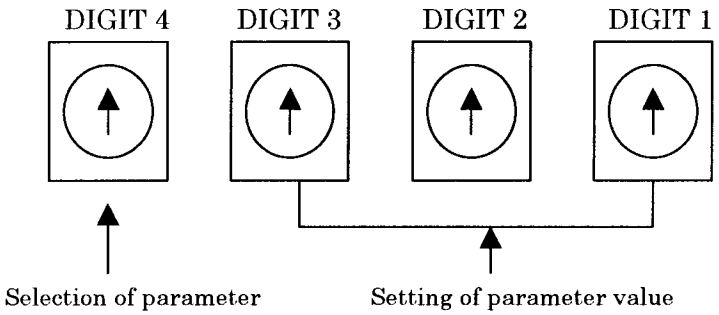
PIN DESIGNATION AND DESCRIPTION

Pin#	Designation	Description
1	C0	BCD SW Digit #1 select signal , low active output pin for parallel data input.
2	C1	BCD SW Digit #2 select signal , low active output pin for parallel data input.
3	C2	BCD SW Digit #3 select signal , low active output pin for parallel data input.
4	C3	BCD SW Digit #4 select signal , low active output pin for parallel data input.
5	TXD	Serial data TX data pin. TTL/CMOS level. Keep open when not used
6	RXD	Serial data RX data pin. TTL/CMOS level. Keep open when not used
.7	/EXT	Connect to GND in case using external reference clock. Internally pulled-up, keep open when internal 8MHz reference clock is used.
8	CLK	Input pin for external reference clock. TTL/CMOS
9	GND	GND of power supply and signal
10	OUT2	TTL/CMOS signal output for 4.5MHz – 60MHz
11	GND	GND of power supply and signal
12	GND	GND of power supply and signal
13	OUT1	Output for 18MHz – 240MHz. Output impedance is 50Ω.
14	GND	GND of power supply and signal
15	+5V	Power supply pin. Supply +5v ±5%
16	PDENB	Phase comparator control pin. Internally pulled-up, VCO is in free-run condition when connected to GND. Open for normal operation.
17	/SET	BCD SW scan starts when this pin is set to low in parallel date mode. BCD SW values are read and set to UPL-240.
18	D0	BCD SW BIT 0 data input pin. This pin is internally pulled-up. Keep open when not used.
19	D1	BCD SW BIT 1 data input pin. This pin is internally pulled-up. Keep open when not used.
20	D2	BCD SW BIT 2 data input pin. This pin is internally pulled-up. Keep open when not used.
21	D3	BCD SW BIT 3 data input pin. This pin is internally pulled-up. Keep open when not used.

■ How to set parameter

(1) Setting by parallel data

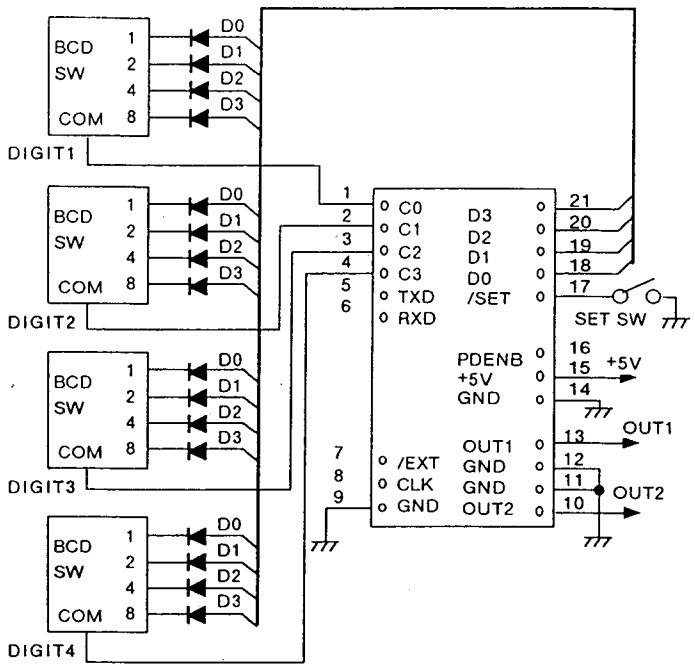
Connect UPL-240 to 4 BCD SW. See Figure 2. Select parameter by DIGIT 4, And set the value for DIGIT 1-3. Push SET SW and the data is set to UPL-240.



DIGIT4 (In hex)	PARAMETER	SETTING VALUE(DIGIT1-3)
0	main divider ratio	Set the value of 65-2047(041-7FF hex)
1	reference clock divider ratio	Set the value of 1-1023(001-3FF hex)
2	Selection of the output phase	Select the output phase of OUT2 Set the value of 0-3(xx0-xx3 hex). Output phase will be changed according to the setting value as Figure 5
3	Fine phase control	Adjust a fine output phase of OUT2. Set the value of 0-14(xx0-00E hex). Setting value and phase delay is changed as Table 1, Figure 4.
4	Selection of phase comparator edge	Select the phase comparator edge of OUT2 and comparator signal. Setting value is 0 or 1(xx0-001hex) Refer to Figure 5.
A	Memory of setting value	Store the above parameters into EEPROM of UPL-240. Set Digit 1 to "1"

When the internal reference clock is used, ignore the above 2,3 and 4.

Figure 2 Circuit example for parallel data



(Remarks)Use the hexadecimal complimentary type for BCD SW. Use general purpose silicon switching diode.

(2)Setting by serial data

In order to set the frequency using a asynchronous serial data, refer to serial data format shown below. When UPL-240 received the data correctly and complete the frequency setting, it returns "*" code (2A hex) as a prompt. When the received data format is not valid or some errors occurred during the transfer, it returns "INVALID DATA". All received data RXD is echo-backed to TXD. Flow control is not provided especially, however, there is no problem in transferring the data continuously.

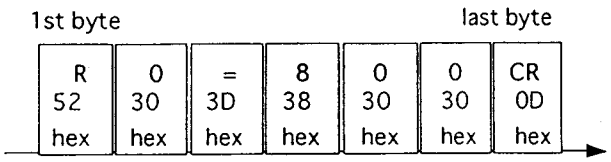
Data Format

Code to be transferred should be used ASCII code.

2-1 How to set main divider ratio

R0=xxxx For xxxx, set the value of 65-2047 in decimal.

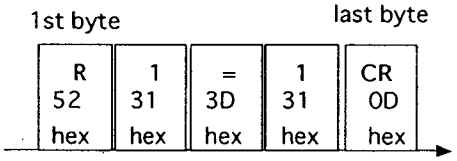
Here shows how to set main divider ratio 800, for example.



2-2 How to set reference clock divider ratio

R1=xxxx For xxxx, set the value of 1-1023 in decimal .

Here shows how to set reference clock divider ratio 1, for example.

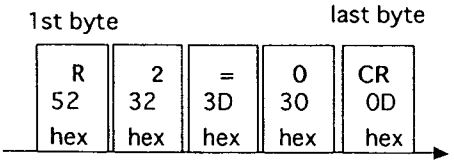


2-3 How to set output phase (for OUT2)

R2=x For x, set the value of 0-3 in decimal.

Refer to the Figure 4 about the relations of setting value and output phase.

Here shows how to set output phase 0° , for example.

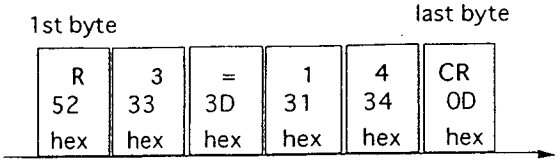


In case of using the internal reference clock, ignore this setting.

2-4 Fine phase control(for OUT2)

R3=x For x, set the value of 0-14 in decimal.

Refer to the Table 1 and Figure 5 about the relations of setting value and output phase. Here shows how to set the delay in order to control fine phase.

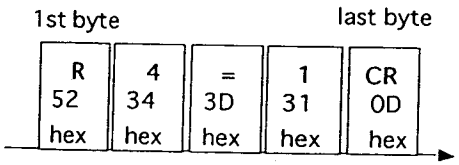


In case of using the internal reference clock, ignore this setting.

2-5 Selection of phase comparator edge (for OUT2)

R4=x For x, set the value of 0 or 1 in decimal.

In case setting 0, the phase comparator uses rising edge., and in case of setting 1, the phase comparator uses falling edge to compare reference and output(OUT2) signals. Here shows how to set rising edge of phase comparator.



In case using the internal reference clock, ignore this setting.

2-6 How to memorize the setting value

RA=1

In order to memorize the above 1-4 parameter into the built-in EEPROM, transfer "RA=1".

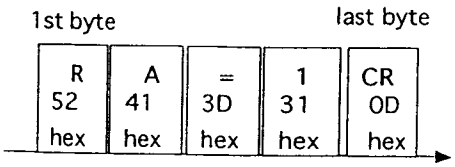
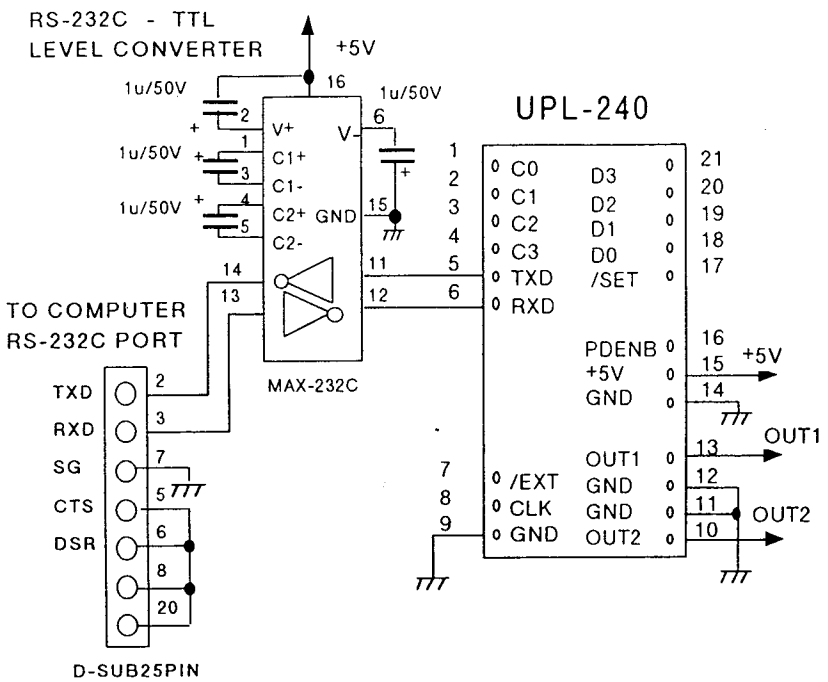


Figure 3 Circuit example for serial data



(Cautions)

(1) In order to get lower phase jitter of output signal, use the comparator frequency more than 100KHz. Note that the comparator frequency is higher, the output signal jitter comes less.

(2) UPL-240 is CMOS device. Pay attention for static discharges.

■ How to control fine phase for output signal

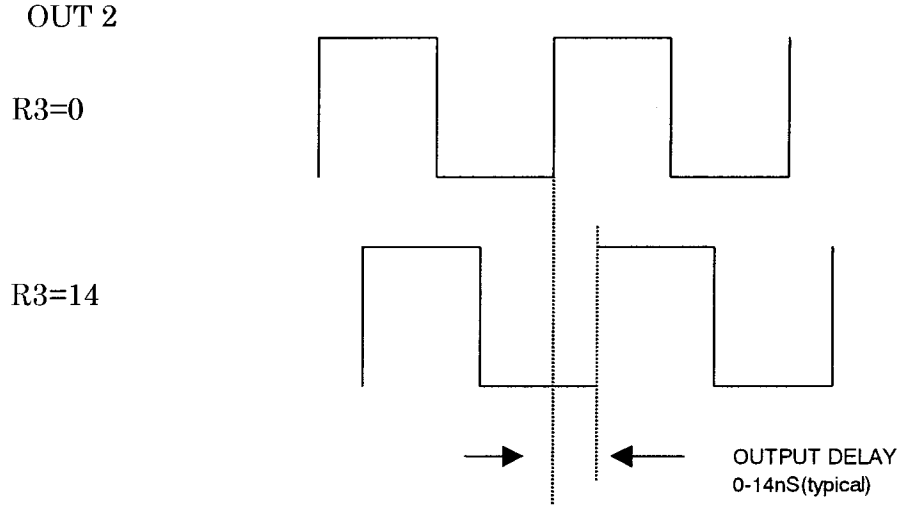
It is possible to control fine phase for output signal.

The following Table 1 shows the relations between the setting value and delay.

Table 1 Relations between setting value of fine control and phase delay

Setting value (hexadecimal)	Setting value (decimal)	Delay(nS) (TYPICAL)
0	0	0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
A	10	10
B	11	11
C	12	12
D	13	13
E	14	14

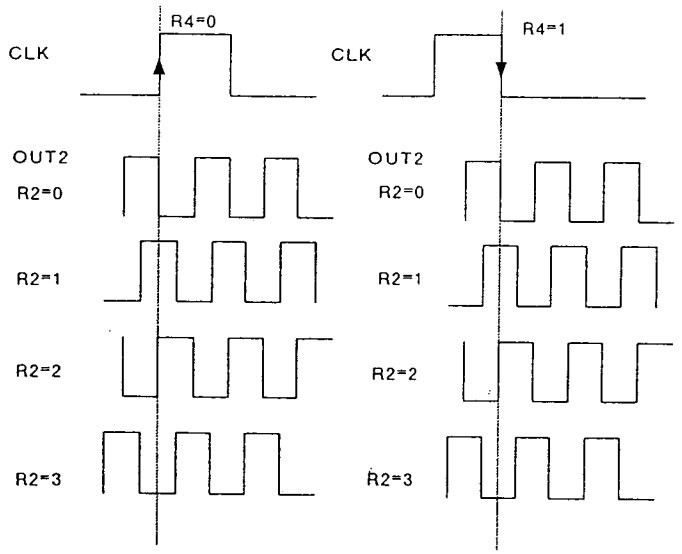
Figure 4 Direction of phase delay



■ Phase relation of output signal

UPL240 can control OUT2 output phase in 90° step. In combination with comparator edge, phase relationship between OUT2 and reference signal is shown below.

Figure 5 Phase relation of output signal



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