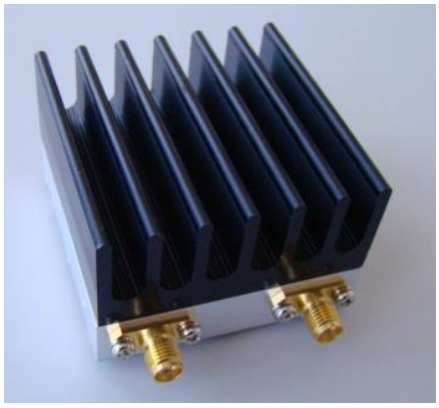
User's Manual

Frequency Synthesizer

DPL-6GF

DPL-6GFH(with Heat Sink)



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Contents

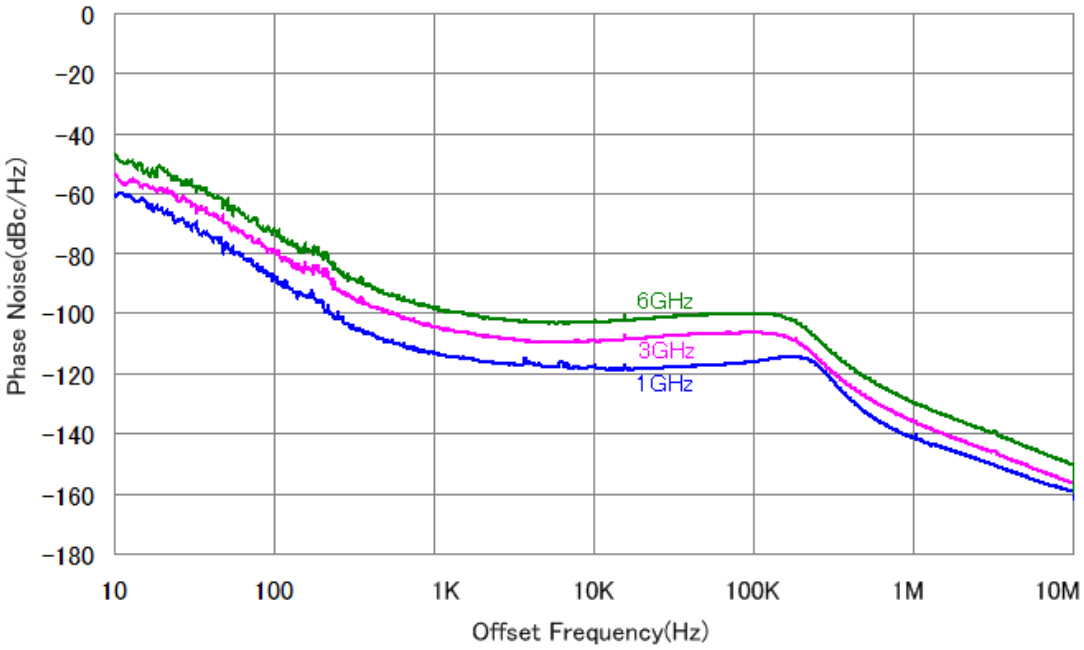
1.General Description

The DPL-6GF is a signal generator module which can set frequency from 50 MHz to 6 GHz. The DPL-6GF generates a signal from 50 MHz to 3 GHz internally by PLL, and the signal from 3 GHz to 6 GHz is doubled using PLL multiplier.
The output of PLL is of a rectangular wave, therefore, frequency of 50 MHz to 3 GHz, a low-pass filter is required for harmonic elimination.
When outputting a multiplied signal from 3 GHz to 6 GHz, a band pass filter is required because of the existence of sub-harmonics and harmonics.
For this reason, specify the frequency you desire in advance before placing an order.
The frequency bandwidth meeting the specification is approximately ±10% of the specified frequency. Furthermore, when no output filter is selected as an option, a programmable output in a 1 KHz step is allowed in a broad band from 50 MHz to 3 GHz (No longer a sine wave).
Note) The frequency bandwidth depends on the cutoff frequency of the filter, however, the cutoff frequency of the filter which you can select is limited. Thus, the frequency bandwidth may drop to below ±10% of the specified frequency therefore, confirm the frequency before placing an order.

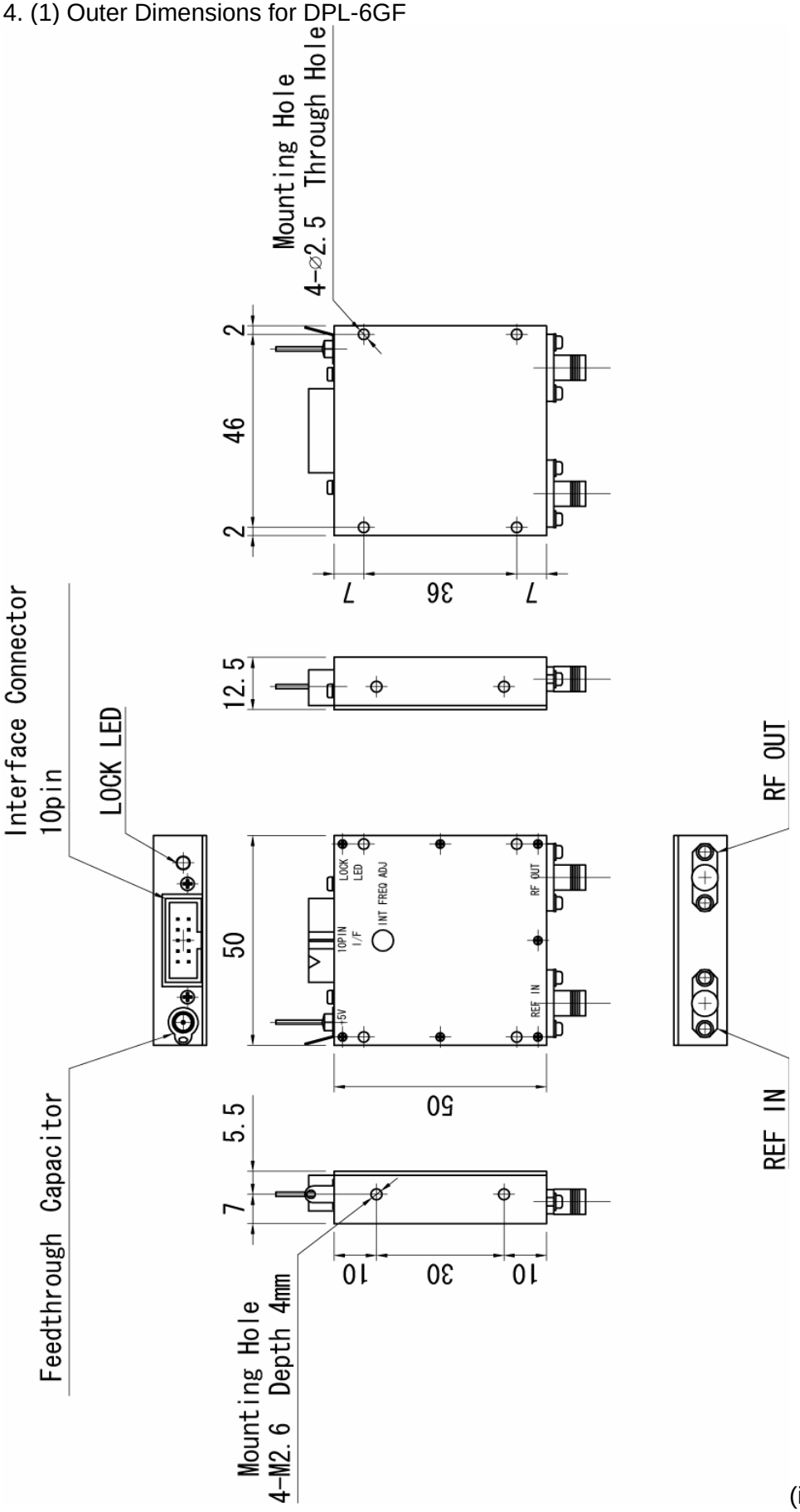
2. Electrical Specification

Power Supply/Current	+5V+/-5%, <600mA
Frequency Range	50MHz-6GHz (approximately +/-10% of the specified frequency
Frequency Resolution	
50MHz-3GHz	1KHz step
3GHz-6GHz	2KHz step
Output Level	>+10dBm
Output Impedance	50 ohm
Spurious	<-65dBc
Harmonics	<-40dBc (in case of no output filter option : <-8dBc)
Phase Noise (typical)	
@6GHz	-80dBc/Hz@100Hz -97dBc/Hz@1KHz -102dBc/Hz@10KHz -99dBc/Hz@100KHz -126dBc/Hz@1MHz
Internal Reference Clock Accuracy	<+/-15ppm 0 - +50 degree C
External Reference Clock and Level	10MHz -6dBm - +6dBm
Lock Time	Max 40msec
Operating Temperature Range	0 - +50 degree C (In case of being installed with thermal resistance 6.5(degree C/W) heat sink
Outer Dimensions	50mmx50mmx12.5mm 50mmx50mmx33.5mm(with Heat Sink)
Interface	(1) Asynchronous Serial Communication 9600bps, 8bits, one stop bit, non-parity 3.3V CMOS level (2)SPI serial communication 3 bytes data 3.3V CMOS level

3. Phase Noise

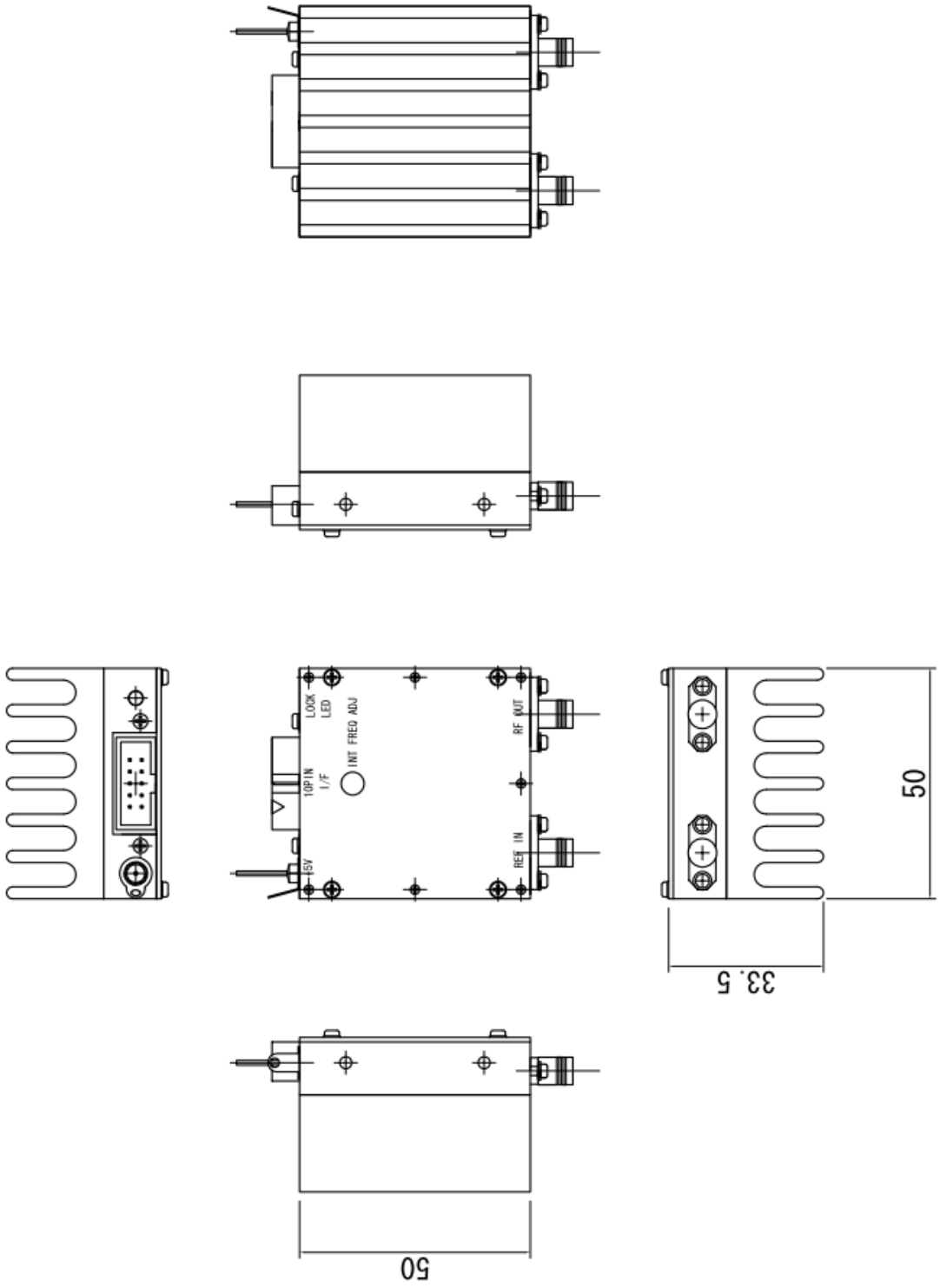


4. (1) Outer Dimensions for DPL-6GF



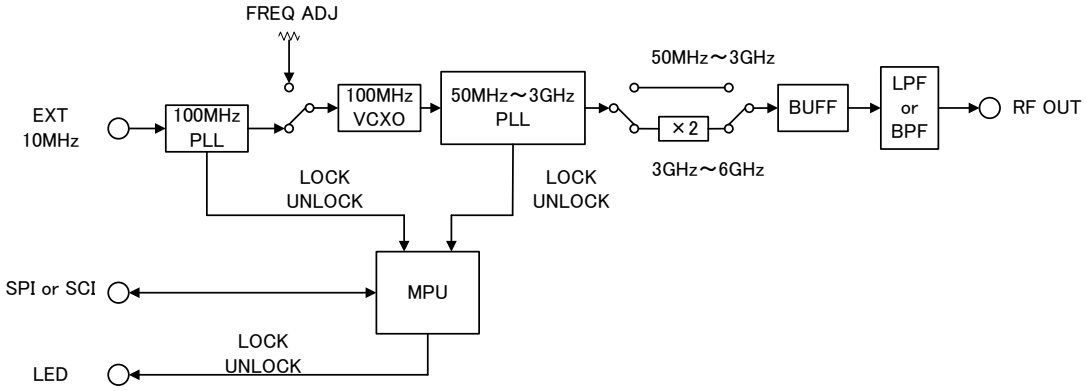
(in mm)

(2) Outer Dimensions for DPL-6GFH



(in mm)

5. Circuit Configuration



6. Connector, Interface

(1) External 10MHz input	SMA-J	50Ω
(2) Output Connector	SMA-J	50Ω
(3) Power Supply Pin	Feedthrough Capacitor	Supply +5V
(4) I/F Connector	2.54mm 5x2 10 pin Connector for Flat Cable Part No. HIF3FC-10PA-2.54DSA(HIROSE)	

Pin Assignment

Pin No.	Name	Description
1	GND	signal GND
2	GND	signal GND
3	POWER SUPPLY	Power input +5V Connected to feedthrough capacitor Internally
4	INT/EXT	Mode selection pin External or Internal Ref clock High: Internal low: External Internally pulled up
5	LOCK	PLL lock status output High: Lock low: Unlock 3.3V CMOS
6	/CS	Chip select under SPI mode Input low active 3.3V CMOS Internally pulled up
7	RXD	Asynchronous serial RX Data 3.3V CMOS Internally pulled up
8	SDI	Serial data input under SPI mode 3.3V CMOS
9	TXD	Asynchronous serial TX Data 3.3V CMOS
10	CLK	Serial input under SPI mode 3.3V CMOS

7. Thermal Consideration

Power dissipation of this module is about 3 watts, so in order to flow heat, mount this module on chassis firmly. Or installing heat sink of heat resistance less than 6.5(degree C/W) is recommended.

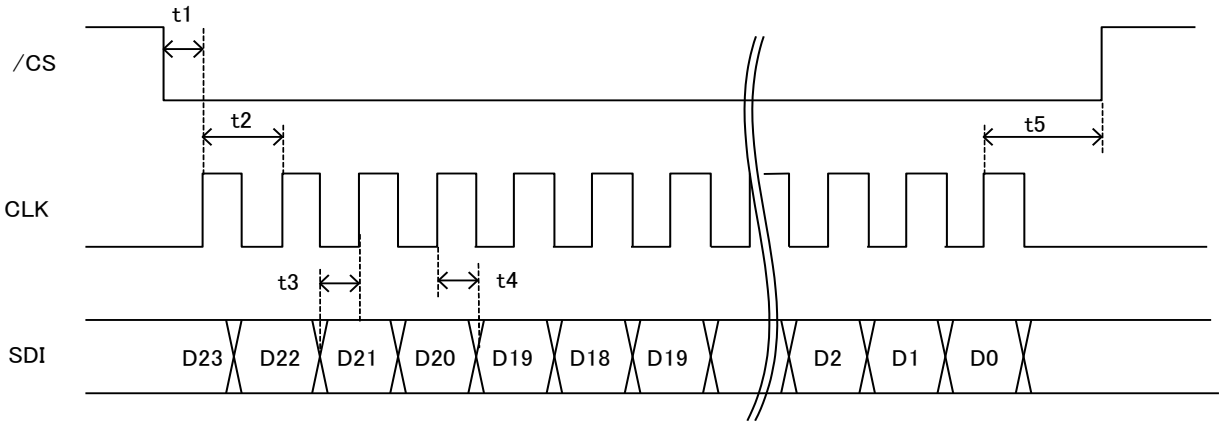
Refer to Page 3 Outer dimensions about mounting holes. It will be more effective if silicon compound is put on the surface of the mounting section of the module.

8. Control by SPI serial data

（1）SPI specification

Max. clock speed	500KHz
Data bits width	24bits (22bits frequency data bits, 2bits reserved)
Logic level	3.3V CMOS

（2）Timing characteristic



Timing characteristic

Parameter	Condition	Min.	Unit
t1	CLK setup time to /CS	50	ns
t2	CLK period	2	us
t3	SDI setup time to CLK rise edge	100	ns
t4	SDI hold time to CLK rise edge	100	ns
t5	/CS set up time to CLK rise edge	50	ns

（3） Command definitions

24 bits frequency data is transferred by serial data.

Actual frequency data bits are 22 bits among 24 bits, the remaining 2 bits are not used. Bit definition is as follows.

Bits	Name	Width	Description
bit[23:22]	Reserved	2 bits	Not used, do not care
bit[21:0]	Frequency	22 bits	Frequency data in 1 KHz resolution in binary

For example, if you set 6GHz, frequency data of KHz unit must be converted to binary data. 6GHz is converted to 5B8D80(hex) in 22 bits binary data.

※ Please note that even if the frequency of beyond 50MHz to 6GHz was set, it would be accepted but the quality of the signal would not be guaranteed.

9. Control by Asynchronous serial data

How to set from a PC serial port(RS-232C) is explained below.

9-1. Communication specification

Speed	9600bps
Data bits	8 bits
Stop bits	1 bit
Parity	None
Flow control	None
Logic level	3.3V CMOS level

9-2. RS-232C connection

The logic level of DPL-6GF serial communication is 3.3V CMOS, which cannot be directly connected to RS-232C level like PC serial port. Level converter(LVC-232C) between RS-232C and 3.3V CMOS is needed. LVC-232C is available from our products line-up. Refer to our Web site

www.dst.co.jp/dcms_media/other/DSTE_LVC-232C.pdf

9-3. Command definitions

Character strings marked as double quotation marks " " means ASCII code, and CR and LF, which are control codes, means 0D(hex) and 0A(hex). If any invalid command is entered, "INVALID DATA" CR LF"*" is returned. All characters used for input should be uppercase. If a normal command is entered, "*" is returned. Also the entered data is echoed back.

9-3-1. Frequency setting command

For frequency setting, input can be made in MHz, KHz and Hz unit.

(1) Setting in MHz

For setting 2400MHzm input the following data.

"2400M"CR

In this case, all the data below 100KHz is set to "0".

(2) Setting in KHz

For setting 2400002KHz, input the following data.

"2400002K"CR

Also the following expression is allowed.

"2400002"CR

※ Please note that even if the frequency of beyond 50MHz to 6GHz was set, it would be accepted but the quality of the signal would not be guaranteed.

9-3-2. READ command

By entering "READ"CR, the currently set frequency is output.

The response is as shown below.

"ffffffffKHz"CR LF

"fffffff" is the frequency of currectly outputting in KHz unit.

9-3-3. SAVE command

By entering "SAVE"CR, the current frequency can be memorized into EEPROM, When the power is on next time, the stored data can be output.

If any invalid command is entered, "ERROR"CR LF"*" is returned.

10. Shipping inspection

100% inspection shall be performed for the electrical specification in 2-1.

11. Warranty

If any defect is found due to the manufacturer's improper production or design within one year after delivery, repair or replacement shall be performed a the manufacturer's responsibility. Digital Signal Technology, Inc. assumes no liability for damages that may occur as a result of handling by users even though the warranty period.

12. Others

11-1. This product, which employs a CMOS device may be easily damaged by static electricity. Digital Signal Technology, Inc. assumes no liability for damages that may occur as the result of handling by users even though the above warranty period.

11-2. Do not supply over voltage power supply, module may be damaged. DS Technology, Inc assumes no liability for damages that may occur as the result of handling by users even though the above warranty period.