

**EPLO**  
**Fixed Frequency Signal Generator**  
**User' s Manual**

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## 1. Function description

EPLO is a signal generator utilizing PLL(Phase Locked Loop) technique. It provides a pure sine signal within the range from 10MHz to 4400MHz. Output options such as LVDS, CMOS sine wave 90 degree phase difference two outputs are available for your convenience. Less+10dBm or over +10dBm output level can be also available as an option. High accuracy external reference clock can be used to improve frequency stability.

It is a compact size and easy to use. To supply 5V single power supply is only thing you have to do.

## 2. Electrical specification

Output wave	sine wave(standard)
Output impedance	50 Ω
Output frequency range	10MHz – 4400MHz
Output level	+10dBm +/- 2dBm(standard)
Spurious level	-60dBc
Harmonic spurious	-30dBc
Internal clock frequency accuracy	+/-2.5ppm(10MHz)
Operating temperature range	0 – +50 degree
Power supply/current	less than +5V+/-5%, 50mA-180mA Less than 300mA(In case high output level option)
Dimensions	50x75x13mm (WDH)

## 3. Option specification

3-1.Output option: 5V-TTL(10M-200M) / 3.3V-TTL(10M-200M)  
/ LVDS(10M-1500M)

### Sine wave 2 outputs (90 degree )

220M-470MHz(QCN-3+, phase difference MAX 8 degree )

330M-580MHz(QCN-5+, phase difference MAX 8 degree )

425M-675MHz(QCN-7+, phase difference MAX 8 degree )

450M-750MHz(QCN-8+, phase difference MAX 8 degree )

800M-1250MHz(QCN-12A+, phase difference MAX 5 degree )

1100M-1925MHz(QCN-19+, phase difference MAX 4 degree )

1350M-2450MHz(QCN-25+, phase difference MAX 5 degree )

1700M-2700MHz(QCN-27+, phase difference MAX 6 degree )

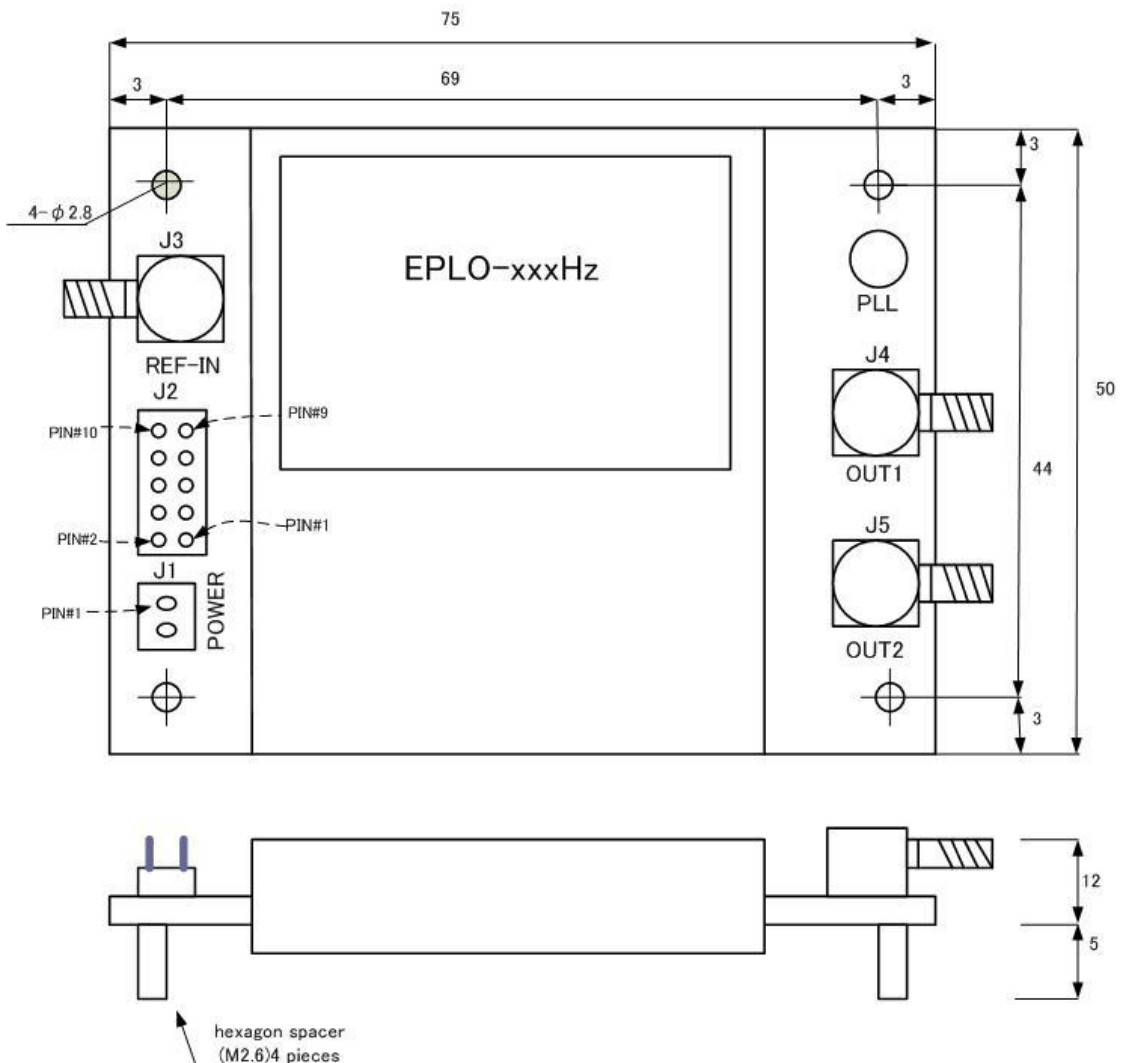
2500M-3400MHz(QCN-34+, phase difference MAX 4 degree )

2500M-4400MHz(QCN-45+, phase difference MAX 6 degree )

\*\* 10M-220MHz, 750M-800MHz not acceptable

- 3-2. Output level:  $-10\text{dBm} - >+10\text{dBm}$
- 3-3. High output level:  $<+10\text{dBm} - +20\text{dBm}$   
 $<+10\text{dBm} - \text{max } +17\text{dBm}$  more than 3500MHz
- 3-4. Output clock input: 10M-100MHz  
 $+0\text{Bm} - +10\text{dBm}$   
 \*\* Square wave : more than 0.6Vp-p needed  
 (50  $\Omega$  terminal)  
 \*\*Sine wave : more than +6dBm needed  
 (50  $\Omega$  terminal)
- In case low reference level, the phase noise performance will be degraded.
- 3-5. External clock input impedance : High impedance(standard) or 50  $\Omega$  possible

#### 4. Outline



## 5. Type of connector and description

### (1) J1: 2.54mm pitch 2 pin connector

If required, it may be mounted for power supply by users,  
when J2 10 pin header is not used.

- Pin function

1: power supply +5V

2: power supply GND

### (2) J2: 10 pin header

- Pin function

1: power supply +5V

2: reserved

3: power supply +5V

4: reserved

5: PLL unlocked signal

6: reserved

HI level (+3.3V) = unlock

7: power supply GND

8: reserved

9: power supply GND

10 : reserved

\*\* Do not connect anything on the above pin 2, 4, 6, 8, 10 to avoid the damages.

### (3) J3 : SMA type

For external REF input option

### (4) J4 : SMA type

For RF output-----sine wave (standard)

For output option -----5V-TTL, 3.3V-TTL, LVDS(+),

sine wave 2 outputs (0 degree )

### (5) J5 : SMA type

Output option----- LVDS(-), sine wave 2 outputs (90 degree )

### (6) LED

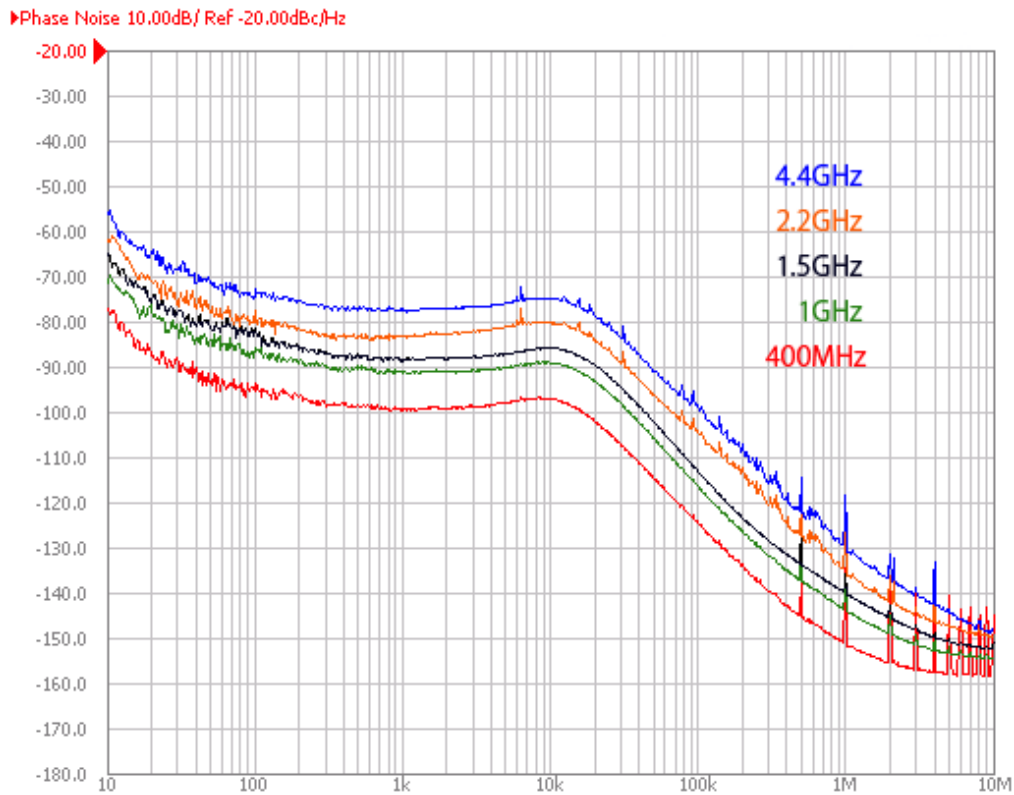
Lock status of PLL

Lock = lighting

Unlock = blinking

## 6. Phase Noise (typical)

Measurement condition : sine wave output with internal reference clock.



### ■ Cautions

Use low noise power supply. When the switching power supply is used, use a noise filter to reduce switching noise from the power supply.

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