Programmable Frequency Synthesizer

Frequency Converter

PCV-50F

Features

- Wide band (0.001Hz～50MHz), High resolution (0.001Hz)
- Converted by any external clock from 7MHz to 50MHz
- Single power supply +5V
- Frequency control by parallel and serial data
- Frequency stored in non-volatile memory
- Low phase noise
- Compact

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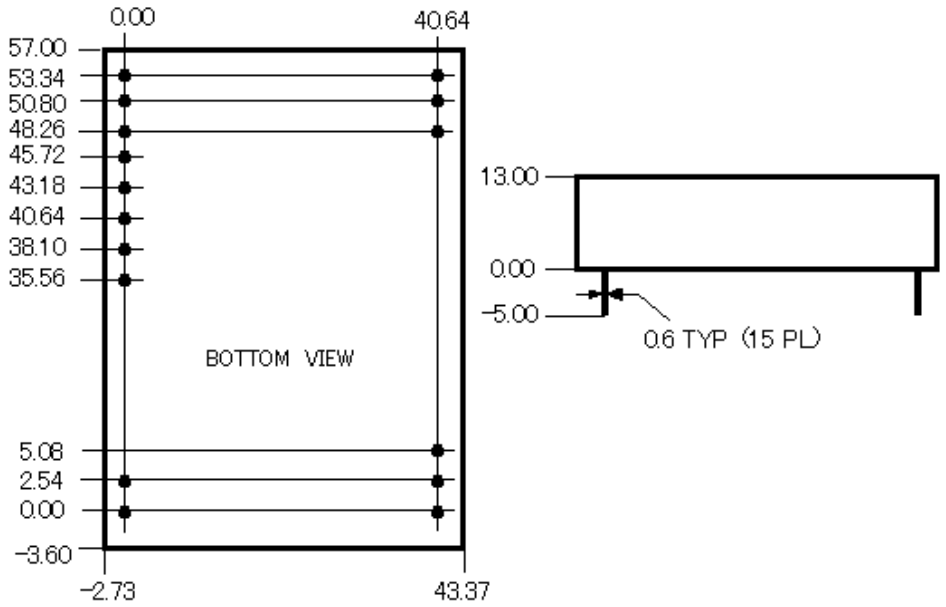
Specifications

Output level	CMOS	
Output frequency range	0.001Hz～50MHz	
Frequency resolution	1mHz (0.001Hz)	
Output waveform duty	50% +/−5%	
Frequency error	0.46 μ Hz or less with respect to external reference	
Jitter	+/−100pS rms or less	(Cycle-to cycle jitter value at 5MHz or higher frequency)
Spurious level	40dBc or more	(excluding harmonics)
External reference signal frequency	7MHz～50MHz	
External reference signal level	2～5Vp－p	DUTY 50±10%
External reference input impedance	470Ω or more	
Frequency control	Parallel input Six signal lines	4-bit BCD input 1-bit digit/data selection 1-bit reference/output frequency Data selection 1-bit strobe signal
	Serial input	9600bps, 8 bits No parity, 1 stop bit
Frequency setting time	Within 250mS (Time between completion of setting of frequency data and acquisition of the set frequency)	
Operating temperature range	0 ～ 50 ℃	
Outer dimensions	61 x 46 x 13 (mm)	
Power supply voltage	+5V+/−5% Consumption current 500mA or less	

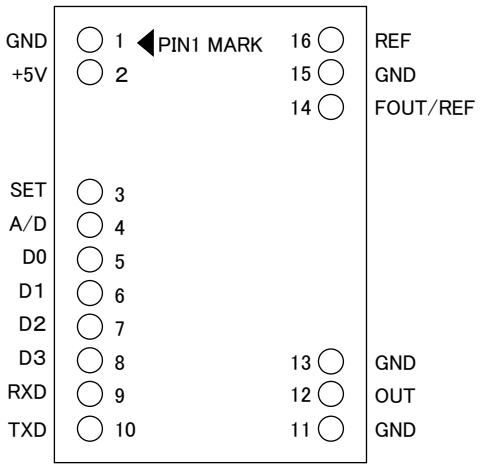
Option

Frequency setting board FIX-PCV50

Outer dimensions



Pin assignments



(TOP VIEW)

Pin names and descriptions

Pin No.	Name	Description
1	GND	Power supply/signal GND
2	+5V	Power supply pin, to which +5V±5% should be supplied.
3	SET	Strobe signal for setting with parallel data. As it is pulled up internally, data of A/D and D0 to D3 are read internally by connecting it to GND. Data is loaded on falling edge.
4	A/D	Select digit or numerical value for parallel data D0 to D3. Set digit of 7-digit frequency data you want to change by H (open). Set the numerical value for selected digit by L (short-circuited to GND) It is pulled up internally.
5	D0	Input of frequency data digit or numerical data bit 0 (2^0)
6	D1	Input of frequency data digit or numerical data bit 1 (2^1)
7	D2	Input of frequency data digit or numerical data bit 2 (2^2)
8	D3	Input of frequency data digit or numerical data bit 3 (2^3)
9	RXD	Asynchronous serial data input pin. Level is TTL-compatible CMOS. When not in use, open it because the input is pulled up.
10	TXD	Asynchronous serial data output pin. Level is TTL-compatible CMOS. When not in use, open it.
11, 13,	GND	Power supply/signal GND
12	OUT	Output terminal
14	FOUT/REF	Input pin to select input of output frequency or reference signal frequency data for frequency setting in parallel: H (open) and L (short-circuited to GND) result in selection of output frequency and reference signal frequency, respectively.
15	GND	Power supply/signal GND
16	REF	Desired external clock input

Remark: Pin No. 3,4,5,6,7,8,9, and 14 are pulled up by 10KΩ